Welcome

Jose Cano, Global Head of Investor Relations
Forward-Looking Statement

Certain statements included herein may constitute forward-looking statements within the meaning of the securities laws of certain jurisdictions. Certain such forward-looking statements can be identified by the use of forward-looking terminology such as “believes”, “expects”, “may”, “are expected to”, “intends”, “will”, “will continue”, “should”, “would be”, “seeks”, “anticipates” or similar expressions or the negative thereof or other variations thereof or comparable terminology. These forward-looking statements include all matters that are not historical facts. They include statements regarding Alphawave IP Group Plc’s (“Alphawave IP”) intentions, beliefs or current expectations concerning, amongst other things, its results in relation to operations, financial condition, prospects, growth, strategies and the industry in which it operates. By their nature, forward-looking statements involve risks and uncertainties because they relate to events and depend on circumstances that may or may not occur in the future. Forward-looking statements are not guarantees of future performance and Alphawave IP’s actual results of operations, financial condition, and the development of the industry in which it operates, may differ materially from those made in or suggested by the forward-looking statements contained in this Presentation. In addition, even if Alphawave IP’s results of operations, financial condition, or the development of the industry in which it operates are consistent with the forward-looking statements contained in this Presentation, those results or developments may not be indicative of results or developments in subsequent periods. Important factors that could cause those differences include, but are not limited to customer demand, Alphawave IP’s innovation and R&D and technology capabilities, target market trends, industry trends, customer activities and end-market trends, market acceptance of Group technologies; increased competition; macroeconomic conditions; changes in laws, regulations or regulatory policies; and timing and success of strategic actions. These forward-looking statements speak only as of the date of this Presentation. As such, undue reliance should not be placed on forward-looking statements. Other than in accordance with legal and regulatory obligations, Alphawave IP undertakes no obligation to publicly update or revise any forward-looking statement, whether as a result of new information, future events or otherwise.
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<thead>
<tr>
<th>Agenda</th>
</tr>
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<td><strong>Welcome</strong></td>
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<td><strong>Consolidating Our Vision for the Business</strong></td>
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<td><strong>Leading Connectivity Technology for the Age of Exponential Data Growth</strong></td>
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<td><strong>QA Session</strong></td>
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<td><strong>High-Performance IP</strong></td>
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<td><strong>Monetising IP Through Custom Silicon</strong></td>
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<td><strong>Connectivity Products – A New Business Opportunity</strong></td>
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<td><strong>Financial Overview</strong></td>
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<td><strong>QA Session</strong></td>
</tr>
<tr>
<td><strong>Closing Remarks</strong></td>
</tr>
</tbody>
</table>
Consolidating Our Vision For The Business

John Lofton Holt, Founder and Executive Chair
Introducing Our New Brand

- We are now a vertically integrated semiconductor company – bringing IP and silicon to customers
- Continues the technology leadership we built on high-speed connectivity IP
- Maintains the Alphawave brand that customers know and trust
- Builds on the credibility with key foundry partners
- Reflects our diverse, open, dynamic and technology-led culture

2022 Deloitte Technology Fast 50™ and North American Technology Fast 500™
Focused on Delivering Results Since IPO…

Strong Performance of Core IP Business

End Customers\(^1,2\)

<table>
<thead>
<tr>
<th>Year</th>
<th>FY 2017</th>
<th>FY 2018</th>
<th>FY 2019</th>
<th>FY 2020</th>
<th>FY 2021</th>
<th>FY 2022</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count</td>
<td>1</td>
<td>1</td>
<td>4</td>
<td>11</td>
<td>20</td>
<td>69</td>
</tr>
</tbody>
</table>

Cumulative Bookings\(^2\) (US$m)

<table>
<thead>
<tr>
<th>Year</th>
<th>FY 2017</th>
<th>FY 2018</th>
<th>FY 2019</th>
<th>FY 2020</th>
<th>FY 2021</th>
<th>FY 2022</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amount</td>
<td>5</td>
<td>10</td>
<td>27</td>
<td>102</td>
<td>347</td>
<td>&gt;580</td>
</tr>
</tbody>
</table>

Revenue (US$m)\(^2\)

<table>
<thead>
<tr>
<th>Year</th>
<th>FY 2018</th>
<th>FY 2019</th>
<th>FY 2020</th>
<th>FY 2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amount</td>
<td>3</td>
<td>11</td>
<td>33</td>
<td>90</td>
</tr>
</tbody>
</table>

Employees\(^2\)

<table>
<thead>
<tr>
<th>Year</th>
<th>FY 2017</th>
<th>FY 2018</th>
<th>FY 2019</th>
<th>FY 2020</th>
<th>FY 2021</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count</td>
<td>28</td>
<td>43</td>
<td>72</td>
<td>154</td>
<td>c.700</td>
<td></td>
</tr>
</tbody>
</table>

Adjusted EBITDA\(^2\) (US$m) & Margin

<table>
<thead>
<tr>
<th>Year</th>
<th>FY 2017</th>
<th>FY 2018</th>
<th>FY 2019</th>
<th>FY 2020</th>
<th>FY 2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amount</td>
<td>36%</td>
<td>26%</td>
<td>59%</td>
<td>58%</td>
<td></td>
</tr>
</tbody>
</table>

Net Operating Cash Flow\(^2\) (US$m)

<table>
<thead>
<tr>
<th>Year</th>
<th>FY 2017</th>
<th>FY 2018</th>
<th>FY 2019</th>
<th>FY 2020</th>
<th>FY 2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amount</td>
<td>5</td>
<td>0</td>
<td>10</td>
<td>19</td>
<td></td>
</tr>
</tbody>
</table>

1 As reported in Q4 2022 trading update. Includes customers from OpenFive who were not already customers of Alphawave and who signed contracts over from 1st September 2022. Revenue generating customers will be reported at FY 2022 results.
2 FY 2017 and FY 2018 as per IPO prospectus.
**...And Investing Capital to Deliver On Expansion Plan**

While Considering Evolving Geopolitics and Uncertain Macro Environment

<table>
<thead>
<tr>
<th>Action</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scale team globally and in UK to maintain technology leadership at 112G and establish 224G lead in new products</td>
<td>Headcount increased from 132 in H1 2021 to c.700 FY2022E</td>
</tr>
<tr>
<td></td>
<td>First successful tape out 3nm</td>
</tr>
<tr>
<td></td>
<td>TSMC OIP Partner 2020-2022 &amp; Samsung Innovation Award 2022</td>
</tr>
<tr>
<td>Land and Expand: Win new customers in new and existing markets, and win new designs at existing customers</td>
<td>From 16 to 28 revenue generating customers (H1 2021 to H1 2022)</td>
</tr>
<tr>
<td></td>
<td>H1 2022: Top 3 customers represented 40% of revenue (excluding WiseWave)</td>
</tr>
<tr>
<td>Expand growth globally, including key high-growth regions such as China</td>
<td>Increasing weight from North American customers in pipeline</td>
</tr>
<tr>
<td></td>
<td>Evolving go-to-market strategy in China</td>
</tr>
<tr>
<td></td>
<td>Future exit of WiseWave JV</td>
</tr>
<tr>
<td>Expand subscription and royalty revenue streams</td>
<td>3 large customers with subscription deals</td>
</tr>
<tr>
<td></td>
<td>Monetising IP via silicon opportunities</td>
</tr>
<tr>
<td>Address emerging chiplet market with chiplet IPs and eventually, manufactured chiplets</td>
<td>Custom silicon and advanced packaging expertise (OpenFive)</td>
</tr>
<tr>
<td></td>
<td>Accelerated transition – vertically integrated (hybrid business)</td>
</tr>
</tbody>
</table>
The Long-Term Vision at IPO

Driving long term scale through layered business models

Illustrative Revenue Mix

- Chiplets (IP and Fully-delivered products)
- Royalties
- Core and Product IP Licensing

Yesterday  Today  Future
Leading Connectivity Technology for Digital Infrastructure

Vertically Integrated - Monetising our IP Through IP Licence and Silicon

IP Licence Business

Vertically Integrated – IP Licence and Silicon

US$300m multi-year agreement with leading North American hyperscaler

Illustrative Revenue Mix

Connectivity Products

Custom Silicon

Chiplets (IP and Fully-delivered products)

Royalties

Core and Product IP Licensing

Pre-IPO

Capital Deployment

Consolidation

Ramp and Scale
Drivers of Our Vision and Ambition

Adapting to External Environment and Stage of Our Business

- Maximising Value For Our Customers
- Expand and Extend Technology Leadership
- Greater Scale

Building a Leading Connectivity Business

- Land and Expand
- High-Performance Silicon IP and Products
- People and culture
- Vertically Integrated
Alphawave’s Commitment to ESG

Building the Team to Support a Responsible Business Expansion

• New hires in 2022 reinforcing our Governance, Finance and Comms functions
• ESG Steering Group to drive improvements and long-term sustainability strategy

Environmental

• Our products contribute to more sustainable data centers
• Fabless business model with relatively lower carbon footprint
• Ongoing commitment to actively manage and reduce our carbon footprint
• Environmental disclosures following TCFD recommendations

Social

• Talent identification and retention programme
• Commitment to Diversity & Inclusion
• Corporate values fostering innovation and the next wave of innovators
• University Relations, Internships, and Community Engagement programme

Governance

• Responsible Company – adhering to high standards as per our Code of Ethics and Business Conduct
• Increasing focus on Supply Chain Governance
• Head of Governance driving further improvements
Leading Connectivity Technology For The Age of Exponential Data Growth
Tony Pialis, Founder and CEO
FY 2022 Bookings

H2 2022 Bookings Reflect Vertically Integrated Business Model

FY 2022 Bookings (US$m)

- 8 new design wins in Q4 2022
- Second design win with opto-electronics products
- Working with 7 of the top 10 semiconductor device companies

US$175m bookings in H2 2022

- US$65m of orders reflect Alphawave’s IP monetised through licence and silicon, up 62% over H2 2021
- Approximately 40% of Licence and NRE bookings in H2 2022 (US$38m) monetise our IP through larger silicon opportunities. This is a reflection of our vertically integrated business model

1 By market capitalisation as of 09.01.23
The Age of Exponential Data Growth

More Sensors, Devices, Images and Multimedia… More Enterprise Data

181 ZB
Size of global datasphere by 2025¹ Data Volume in Zetabytes

1 The Data Center Journey, From Central Utility To Center Of The Universe (semiengineering.com). Source Statista
See slide 93 for all other references
Bandwidth-Limited Data Infrastructure

Connectivity is Struggling to Meet Bandwidth Required for Exponential Growth of Data

Data Rates Double every 2-3 Years

<table>
<thead>
<tr>
<th>Year</th>
<th>Switch data rate</th>
<th>Transceiver data rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>2017</td>
<td>5Tbps x2</td>
<td>100G 4x 25G PAM4</td>
</tr>
<tr>
<td></td>
<td>Ex. 48 ports at 100G</td>
<td>x2</td>
</tr>
<tr>
<td>2020</td>
<td>12.8Tbps x2</td>
<td>200G 4x 50G PAM4</td>
</tr>
<tr>
<td>2022</td>
<td>25.6Tbps x2</td>
<td>400G 4x 100G PAM4 / Coherent</td>
</tr>
<tr>
<td>2025</td>
<td>51.2Tbps x2</td>
<td>800G 4x 200G PAM4 / Coherent</td>
</tr>
</tbody>
</table>

Source: "Silicon Photonics Market and Technology Report 2020", April 2020
Silicon Photonics Market & Technology 2020 - Yole Développement (i-micronews.com)

Top 10 countries by number of data centers in 2022, Statista

> 8.5k data centers worldwide

Cloudscene
Addressable Market Expanding to $18B by 2026

<table>
<thead>
<tr>
<th></th>
<th>2023</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>US$B</td>
<td>10.1</td>
<td>17.6</td>
</tr>
<tr>
<td>Opto-Electronics</td>
<td>3.6</td>
<td></td>
</tr>
<tr>
<td>CAGR (%)</td>
<td>20%</td>
<td></td>
</tr>
<tr>
<td>Custom Silicon</td>
<td>11.9</td>
<td></td>
</tr>
<tr>
<td>CAGR (%)</td>
<td>16%</td>
<td></td>
</tr>
<tr>
<td>High Performance IP</td>
<td>1.1</td>
<td>2.1</td>
</tr>
<tr>
<td>CAGR (%)</td>
<td></td>
<td>24%</td>
</tr>
</tbody>
</table>

**Market Drivers**

- Digitalisation drives exponential growth in data
- Data bandwidth doubles every 2-3 years driving a technology refresh of switches and transceivers
- High-speed and power-efficient connectivity technology is a key enabler
- Hyperscalers investing through the economic cycle

Semico Research Corporation, December 2022, IPNest and Lightcounting
Our Technology Enables High-Speed Data Transmission

In Key Applications Inside Data Centers

Semiconductors are at the start and end points of any transmission of data

<table>
<thead>
<tr>
<th>Applications</th>
<th>Where</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing (Compute)</td>
<td>CPU, GPU, FPGA, AI</td>
</tr>
<tr>
<td></td>
<td>In Servers and AI/ML racks</td>
</tr>
<tr>
<td>Networking</td>
<td>Network cards (NICs), Switch, optical</td>
</tr>
<tr>
<td></td>
<td>modules and cabling</td>
</tr>
<tr>
<td></td>
<td>In servers and AI/ML racks, switches,</td>
</tr>
<tr>
<td></td>
<td>optical modules, and cabling</td>
</tr>
<tr>
<td>Storage</td>
<td>Solid State Drives (SSD), Flash</td>
</tr>
<tr>
<td></td>
<td>Memory, Hard Disk Drives (HDD)</td>
</tr>
<tr>
<td></td>
<td>In storage rack</td>
</tr>
</tbody>
</table>
Alphawave Technology Strengths

Leading Edge Capabilities and Technologies to Deliver the Fastest Connectivity Solutions

High-Speed Connectivity IP
- 224Gbps, 112Gbps, chiplets
- #1 TSMC OIP partner 2020-2022
- 2022 Samsung Best Collaboration Award

Advanced Silicon
- First in 7nm, 6nm, 5nm, 4nm and 3nm

Chiplet – Package Design
- Deep expertise in chiplet packages design
- 2.5D and 3D package designs in production

Opto-Electronics
- PAM4, Coherent DSPs, and silicon photonics for 1.6T Ethernet
- 224Gbps photonics in silicon
Technology Progress Since IPO

112G 7nm  6nm  5nm  4nm  3nm

- **Number of IPs**
  - 2018: 70
  - 2019: 80
  - 2020: >220

- **AresCORE OptiCORE100**
- **9 New IP COREs**

- **Custom Silicon Expertise**
  - 2.5D + 3D packaging
  - Storage IP
  - Optical DSP

- **Progress Through M&A**

- **TSMC OIP Partner 2020**
- **TSMC IOP Partner 2021**
- **Intel IFS IP Founding Partner**
- **PCI-SIG Integrator PCIe Gen5**
- **UCle² Consortium**
- **TSMC OIP Partner 2022**

- **Founding Member TSMC OIP 3D Fabric Alliance**
- **Samsung Innovation Award 2022**

1 Including acquired OpenFive IP
2 Universal Chiplet Interconnect Express Consortium. [https://www.uciexpress.org/](https://www.uciexpress.org/)
Building a Leading Connectivity Business

**High-Performance Silicon IP and Products**
- Leading edge connectivity IP
- Delivering the fastest connectivity solutions
- Complete set of products and expertise aligned to long-term market trends

**Vertically Integrated**
- Monetising our IP through IP licences, custom silicon and connectivity products
- Greater scale
- Enhanced competitive position

**People and Culture**
- Technology-centric, open and diverse culture fosters innovation
- Approximately 700 employees
- Key design centres in Canada, US, Israel and India

**Land & Expand**
- Adding value to customers by servicing more of their connectivity needs
- Growing opportunity with large cloud, wireless infrastructures and hyperscalers
- Collaborative approach with customers promotes innovation
Leading Connectivity IP and Silicon

Vertically Integrated Business Offering Customers a Wide Range of Products/Solutions

Connectivity Silicon IP
- Networking, Optical, Compute, Storage, AI, CPU, 5G Infrastructure, Automotive

Custom Silicon
- Bespoke silicon to customers’ requirements incorporating our Connectivity IP

Connectivity Products
- High bandwidth, advanced node optical and electrical networking products

> 220 IPs and partnered with TSMC, Samsung, Intel

80 active customers

PAM4 & Coherent Transceivers

Leveraging our IP
## Connectivity IP Group

<table>
<thead>
<tr>
<th>Servers and Storage</th>
<th>Networking</th>
<th>Memory</th>
<th>Chiplets</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-speed Interface IP for data centre compute – CPU, GPU, AI &amp; FPGA</td>
<td>Interface IP for Networks – Switches, Routers, DPUs, NICs</td>
<td>Memory Interface IP for DRAMs &amp; HBM – CPU, GPU, AI, FPGA, DPUs</td>
<td>Chiplet Interface IP 2.5D and 3DIC</td>
</tr>
</tbody>
</table>

### Servers and Storage
- PCIe Gen6 / CXL 3.0

### Networking
- 400G, 800G, 1.6T Ethernet

### Memory
- HBM, LPDDR, DDR

### Chiplets
- UCIe, BOW, Open-HBI

**IP Core Examples**
Custom Silicon Group

Silicon Proven Solutions Leveraging Our High-Performance IP

Custom Silicon Expertise
- Experienced engineering teams and advanced packaging expertise (2.5/3D)
- Reliable operations and partnerships
- Proven design flow and methodology for leading nodes
- Application optimized IP sub-systems

Synergistic Model

Silicon IP
- >155 IPs and partnered with TSMC, Samsung, Intel
  - PCIe/CXL
  - 224G/112G
  - Ethernet
  - HBM, LPDDR, DDR
  - Die-to-Die – Chiplets
  - RiscV

Complete Solution

Strong Partnerships Across the Supply Chain

EDA/IP
- ARM
- Cadence
- CEVA
- Rambus
- SiFive
- Synopsys

Manufacturers
- TSMC
- Samsung
- Intel
- GlobalFoundries
- Synopsys

Package and Test
- ASE Group
- Signetics
- Kyocera
- ISE Lab, Inc.
Connectivity Products Group

Full Range of PAM4 and Coherent DSPs – Electrical and Optical

Electrical cables are used within the rack.

Optical coherent signalling is used today, to connect regional data centers through optical cables.
Growing opportunity to use coherent inside data centers.

Optical cables distribute data across a data center.
Co-packaged Optoelectronics.

Direct Detect modulation such as PAM4 DSP for speeds up to 200G.

Coherent DSP for longer reaches and for shorter reaches at 200G and above.
Adding Value to Customers - Land & Expand

Servicing More Connectivity Requirements

- Technology refresh/upgrade provide an opportunity to work with new customers
- Once technology is qualified and deployed is easier for customers to increase adoption
- Close R&D collaboration with customers drives product development
- Hyperscaler multi-year agreement provides unique platform to develop new products and scale the business
- More than 120 customers added since 2018

<table>
<thead>
<tr>
<th>Number of End Customers</th>
<th>28</th>
<th>120</th>
</tr>
</thead>
<tbody>
<tr>
<td>H1 2022</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Active customers,</td>
<td></td>
<td></td>
</tr>
<tr>
<td>including 40 IP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>customers and 80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>custom silicon</td>
<td></td>
<td></td>
</tr>
<tr>
<td>customers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>North American</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hyperscaler agreement</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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The Evolution of Data Center Silicon: A Growing Opportunity For Chiplets

N-1 Silicon Designs 16/12/7 nm

- Alphawave IP integrated in compute silicon. One die and one package:
  - > $250M cost of design
  - > 2 years design cycle

- Silicon costs increasing in advanced manufacturing technologies like FinFet

N+1 Silicon Designs 5/4/3 nm

- Alphawave custom silicon expertise the foundation to prebuild connectivity chiplets and optical chiplets

- Delivering connectivity at higher bandwidth and lower power

**Cost effective and flexible approach:** individual chiplet components can be manufactured at different and less expensive nodes and individually replaced
People and Culture

Attracting Talent and Creating an Environment to Foster Leading Innovation

• Welcomed approximately 400 new employees from Precise-ITC, OpenFive and Banias Labs
• Attracting and retaining talent:
  • Employee share ownership aligned to shareholder’s interests
  • Working on leading edge technology
  • Supporting employees’ wellbeing through period of accelerated business expansion
• Technology-centric culture focused on solving the hardest challenges
• Promoting an open and diverse environment to foster innovation
Greater Scale of Vertically Integrated Model

Delivering Accelerated Revenue Growth

• High-growth expanded addressable market accessible by vertically integrated business
• Wider offering of connectivity silicon IP, custom silicon and opto-electronic products focused on data centers and wireless infrastructure
• Supports our long-term ambition of $1 billion revenue run rate by 2027
The Future of Digital Infrastructure

Tony Chan Carusone, Chief Technology Officer
Connectivity – Digital Infrastructure

**Infrastructure Computing and Networking**

- Infrastructure computing and networking are the basis for the modern world:
  - Mobile communication (5G+)
  - Remote work, education, entertainment (Metaverse)
  - AI training (autonomous driving)
  - Scientific computing (chemical and multi-physics simulations: drug discovery, climate change, human brain emulation)

- Data transmission networks account for 1-1.5% of global electricity use\(^1\)

- Data centres and data transmission networks represent about 1% of energy-related greenhouse gas emissions\(^1\)

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1. IEA (2022), Data Centres and Data Transmission Networks, IEA, Paris. See slide 93 for all other references
Data Connectivity Everywhere

Our Expertise is in The Circuits and Systems Required to Communicate Data…

…Whether separated by kilometres of optical fibre or meters of copper cable, sub-millimetre printed wiring, the start- and end-points of data are silicon chips

Inside Data Centers…

• Up to 76% of all data centre internet traffic traverses internally within data centres

…and at the Edge (5G rollout a major driver)

• Placing application-specific compute close to the sources of data
• Creating new applications for high-speed connectivity
Chip-to-chip Connectivity

Our Expertise is in The Circuits and Systems Required to Communicate Data

- Wiring printed on the circuit boards carries the data between chips
- Connectivity between processors (CPU, GPU\(^1\)) and storage is generally PCIe (Peripheral Component Interconnect Express)
- Connectivity between processors and memory is DDR (Double Data Rate) or HBM (High Bandwidth Memory)
- PCIe, DDR and HBM are standardized interfaces

---

\(^1\) CPU: Central Processing Unit; GPU: Graphics Processing Unit
Strong Performance Across a Range of Metrics

Our Solutions Meet the Increasing Requirements of Infrastructure Computing and Networking

**Bandwidth**
Throughput achievable over a single link: data/time
The higher the better

**Latency**
End-to-end travel time for data
Dedicated solutions for applications where (low) latency is critical

**Reach**
The length and attendant signal loss between the start- and end-points of a link
Longer reach allows to eliminate intermediate silicon parts to receive and retransmit

**Density**
Number of transmitters and receivers in a single chip
100’s of parallel streams of data in and out of a single chip

**Power Consumption**
Main operating cost
Impact of heat dissipation on reliability
Low-power modes and flexible power supplies

**Robustness**
Work reliability of the link in every environment
Highly reliable, reconfigurable and adaptive

**Cost**
Smaller chip area = lower silicon cost
Self-test features to keep production test costs low
Key Technology Trends

**Optics Getting Closer to The End Points**
Increasing use of optical cables over copper and co-packaged optics for lower cost, power and latency

**Coherent Optical**
Increasing use of coherent optical communication inside data centers to overcome the bandwidth limitations of optical components

**Disaggregated Computing**
Disaggregation of compute and storage to increase efficiency

**Advances on CMOS Technology**
Higher development and manufacturing costs of high-end semiconductors

**Chiplet**
Emergence of the chiplet design paradigm
Increased Used of Optical Cables For Shorter Reaches

Alphawave Technologies For Both Copper and Optical Connectivity

• Cables connect computers in racks to each other, today mostly copper cables
• Switches route data to other racks, typically over Ethernet links
• In hyperscale data centres, aggregated data traffic flows across longer distances up to a few kilometres
• Increasing data rates is driving a long-standing trend towards the increasing use of optical fibre
• Even short links that were previously copper, are now converting to optical fibre
Co-Packaged Optics – Lower Cost, Power and Latency

- Both optical and electrical links are combined in the network
- Emerging trend towards integration of the optics directly alongside the silicon end-points
- Eliminates the need for intervening receive and re-transmit
- Alphawave is well positioned to benefit from this trend. Our solutions’ reach and robustness eliminate the need for additional re-transmitters.
Increasing Use of Coherent Optical Communication

- PAM4 electrical and optical communication used inside the data center
- Coherent optical communication was traditionally reserved for long-haul, for example connecting data centers across countries
- With increasing data rates, its use has migrated to shorter reaches with a popular coherent standard (400G-ZR) for campus-area networks
- Further cost and power reductions required to bring coherent technology to even shorter-reach applications, such as inside the data center (IDC)
- The acquisition of Banias Labs brings a unique, differentiated and patent-protected technology for low-power, low-cost coherent optical communication
**Disaggregated Computing**

**Increased Efficiency of Storage Capacity Supported by Specialised Connectivity Solutions**

- Sharing memory and storage in centralized pools allows it to be used more efficiently
- Disaggregated model requires specialized low latency connectivity solutions, such as Compute eXpress Link (CXL)
CMOS Fabrication Technology Scaling

- CMOS chip fabrication technology continues to advance
- Alphawave works with the leading foundries who provide the manufacturing capabilities
- Advances in CMOS now allow tremendous computational power on a single silicon die, requiring tremendous connectivity
- Alphawave has consistently been first to provide leading-edge (100 Gbps) connectivity IP in every major new CMOS technology node since its founding from 7nm to now 3nm
- BUT… the cost of integrating compute, connectivity and ancillary functionality on a single die is prohibitive

![Diagram of CMOS technology evolution from 2011 to 2023]
Chiplets Enabled by High-Speed Die-to-Die (Data) Links

Alphawave is at The Forefront of The New Chiplet Design Paradigm

• Chiplets are individual dies that are co-packaged side-by-side. The combination operates and is sold as a single chip

• Relies on a fabric of dense high-speed interconnect

• Wide acceptance of the Universal Chiplet Interconnect Express\(^1\) (UCIe™) standard in 2022 to accelerate and democratize the chiplet ecosystem

• Alphawave is a contributing member in UCIe which defines the standards governing chiplet design and use

• We are a leader in developing both silicon IP for chiplets and complete chiplets for the market

\(^1\) [https://www.uciexpress.org/](https://www.uciexpress.org/)

IO – Input/Output – Data connectivity
Key Technology Trends

**Optics Getting Closer to The End Points**
Technology for both optical and electrical cables

**Coherent Optical**
Coherent Optical In-house with acquisition of Banias Labs

**Disaggregated Computing**
Disaggregation enabled by specialised connectivity solutions

**Advances on CMOS Technology**
Extending technology leadership, from 7nm to 3nm

**Chiplet**
Relies on a fabric of dense high-speed data interconnect
Long-Term Technology Trends

Today

- Emphasis on using copper connectivity wherever possible to keep costs low
- Computer and system designers select packaged electronic parts and wire them together on a custom circuit board
- Global and interconnected supply chain

10 Years

- Ubiquitous use of low-cost optical connectivity solutions, even over short reaches
- Complete systems designed and made by packaging multiple standard silicon chiplets within a few centimetres
- Complete on-shore ecosystem for integrated circuits, chiplets, advanced packaging

Alphawave Semi is well-positioned to:

- Extend and expand technology leadership
- Deliver solutions for emerging optical connectivity
- Offer complete custom silicon expertise and chiplet IP
- Leverage solid relationships with major western companies and governments
15 Min. Break
## Agenda

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<th>Presenter</th>
</tr>
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<td>Jose Cano, Head of Investor Relations</td>
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<td>Consolidating Our Vision for the Business</td>
<td>John Lofton Holt, Founder and Executive Chair</td>
</tr>
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<td>Leading Connectivity Technology for the Age of Exponential Data Growth</td>
<td>Tony Pialis, Founder and CEO</td>
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<td>The Future of Digital Infrastructure</td>
<td>Tony Chan Carusone, Chief Technology Officer</td>
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<td>QA Session</td>
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<td>15 Min. Break</td>
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<td>Jonathan Rogers, Founder and SVP Engineering</td>
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<td>Monetising IP Through Custom Silicon</td>
<td>Mohit Gupta, SVP &amp; GM IP and Custom Silicon</td>
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<td>Connectivity Products – A New Business Opportunity</td>
<td>Babak Samimi, SVP &amp; GM Connectivity Products</td>
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<tr>
<td>Closing Remarks</td>
<td>Tony Pialis, Founder and CEO</td>
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</table>

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High-Performance IP

Jonathan Rogers, Founder and Senior Vice President Engineering
Connectivity IP is the DNA of Our Business

Growing IP Portfolio – Enabling Data to Travel Faster, More Reliably & Using Less Power

• Over 220 connectivity IPs
• Our customers include leading semiconductor companies and hyperscalers as well as internal Custom Silicon and Connectivity Products
• R&D Group develops reusable IP platforms:
  • Allows us to leverage core technologies across the business.
  • Platforms engineered to efficiently support high ROI customization to specific applications.
• Extremely capable team focused cutting edge analog and mixed signal design.
• Very technical and data driven R&D engineering culture that extends from front-line designers all the way up through management.
Increasing Investment in Connectivity Technology

Our Connectivity IP Enables

- Faster Speeds
- Lower Power
- Lower Cost

Silicon IP Megatrends

3rd party silicon IP adoption driven by

- Reduced Cost
- Shorter Time to Market
- Increased Complexity

Continual refresh cycles driven by evolution of

- Standards
- Speeds
- Process Nodes
Addressing High-Growth Digital Infrastructure Markets

IP products offered at 7nm-3nm addressing wide range of digital communication channels

End Markets
- Compute
- Artificial Intelligence
- Data Networking
- Autonomous Vehicles
- 5G Network
- Solid State Storage

Data Center opportunity

Electrical Backplane | Passive Copper Cable | Optical Module DSP | Active Electrical Cables | Active Optical Cables | Chip To Optical Module | Chip To Chip | Co-Packaged Optics | Die To Die
Connectivity IP Group – High-Performance Connectivity IP

**Servers and Storage**
High-speed Interface IP for data centre compute – CPU, GPU, AI & FPGA

**Networking**
Interface IP for Networks – Switches, Routers, DPUs, NICs

**Memory**
Memory Interface IP for DRAMs & HBM – CPU, GPU, AI, FPGA, DPUs

**Chiplets**
Chiplet Interface IP 2.5D and 3DIC

- **PCIe Gen6 / CXL 3.0**
- **400G, 800G, 1.6T Ethernet**
- **HBM, LPDDR, DDR**
- **UCIe, BOW, Open-HBI**
Growing IP Portfolio Inside the Data Center

- AthenaCORE
- ZeusCORE
- ApolloCORE
- OmegaCORE
- AlphaCORE
- OptiCORE100
- AresCORE
- DieCORE
- GammaCORE
- PipeCORE
- HelenaCORE
- DemiCORE
- KappaCORE

IP Cores
- Phy
- Controllers

25 tape-outs in 2022
10 tape-outs in 2021
Unified Configurable DSP IP Platform Powers Our Offerings

The Alphawave IP Configurable Platform

Common Standard Chassis
- Digital Signal Processing (DSP) Engine
- Analog Front-End
- Product Interface

Configurable Options
- Speeds (2.5Gbps – 112Gbps)
- Network protocol (Ethernet, PCIe)
- Number of pins/channels
- Power consumption
- Performance/Reach
- Footprint/size
- Interfacing with Optics

Multiple Product Families and Configurations

- ZeusCORE
- AlphaCORE
- PipeCORE
- ApolloCORE

- Configurable interface IP to deliver products to multiple markets and applications
- Supported by the leading foundries in the most advanced technology
- 1st to silicon in 7nm, to 3nm nodes
- Customer Benefits:
  - Fast time to market
  - Low risk
  - Lower cost products
  - Configurable for wide application use/reuse
Case Study - DSP Transceivers PHY

- Transceiver is a bi-directional digital data communication system.
  - >100 billion bits per second on a wire
  - Located on the edges of all the key silicon communication chips
  - Gets data on and off the chips where the processing occurs
- Transceiver PHY capabilities:
  - Analog front end (AFE)
    - High performance analog to digital converter (ADC)
    - High performance digital to analog converter (D/A)
    - Clock generation
  - Digital signal processing. (DSP)
- Mixture of high-performance analog and digital design activities within the teams creating these IPs.

1 The PHY forms the physical interface and is responsible for coding and decoding of data between a purely digital system and the medium on which the signals are transmitted. It represents a bridge between the digital and electrical connection levels of the interface. PHYs can be discrete components or can also be integrated.
Case Study – Integrated Subsystem

Integrated Ethernet Subsystem Solutions – Faster Go-To-Market

- Combine AlphaCORE DSP transceiver and the OmegaCORE Ethernet Controller
- Pre-validated complete subsystem allows for rapid integration into customers’ SoCs
- Dramatically reduces customer development effort.

![Diagram of integrated Ethernet subsystem]
The R&D group supports three main types of customers:
- IP licensing
- Custom Silicon engagements
- Internal Connectivity Products

Average 12-month engagement - earlier part of customer development:
- IP integration support including simulation and Design For Test
- Package signal and power integrity analysis
- Automated Test Equipment test development

We then support the customer in the production journey.
What is Next?

Leveraging R&D Across The Business

**IP Development**

- Next generation 200Gbs+ DSP Transceiver platform and associated products
- Extending our Integrated Subsystem offering in the PCIe and CXL space
- Enabling a wide variety of chiplet applications with our full portfolio of Transceiver and D2D\(^1\) IP

**R&D Engineering**

- Continue to drive IP licensing business
- Enable higher value Custom Silicon opportunities with our IP
- Provide customized IP platform variants for our connectivity products

---

We have the best R&D team in the industry and this will drive our success

\(^{1}\) Die-to-Die
Monetising Our IP Through Custom Silicon

Mohit Gupta, Senior Vice President and General Manager Custom Silicon and IP
Custom Silicon Group

Delivering High-Quality Custom Silicon for 20 Years

- End-to-end expertise to deliver high-quality silicon in advanced notes
- Strong IP portfolio in memory interfaces & complex package capability
- Proven engineering and silicon operations team
- Offices in US (Silicon Valley), India (Bangalore and Pune) and APAC

300+ employees
80 active customers
14.5 million units shipped in 2022 (cumulative shipped 150m+)
<25 DPPM

1 Defective parts per million
Custom SoC’s – Key Market Segments

- Data Centre Compute
- Data Networking
- Artificial Intelligence
- Solid State Storage
- 5G Network

*Data center opportunity*
Custom Silicon – All about growth

Pushing The Performance Limits for specific use-cases

- Purpose built custom SoCs leveraging high speed connectivity with increasing levels of compute
- Optimized to specific use cases (Youtube servers, Tesla FSD, accelerators for public cloud, etc)
- Deeply tied to software infrastructure

Custom Silicon Addressable Market

US$B

<table>
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<tr>
<th>Year</th>
<th>Value</th>
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<tr>
<td>2026</td>
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Semico Research Corporation, December 2022,
IP Integration at the Core of SoC Design

From Integrated Device Companies… to Fabless Model… to Specialized Design & “IP-less” Era

Common IP Sub-systems With Application Specific Customizations

NETWORKING SWITCH SoC

- ETHERNET SUBSYSTEM
- HOST SUBSYSTEM (PCIE/CXL)
- CUSTOMER SPECIFIC IP
- N/W ACCELERATORS
- MEMORY SUBSYSTEM

ENTERPRISE/DATACENTER STORAGE SoC

- COMPUTE CPU SUBSYSTEM
- HOST SUBSYSTEM (PCIE/CXL)
- CUSTOMER SPECIFIC IP
- AI ACCELERATORS
- ENCRYPTION
- OPTIONAL ETHERNET SUBSYSTEM
- MEMORY SUBSYSTEM

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Benefits of Pre-Built “Application Optimized” IP-Subsystems

Lower Costs And Faster Time to Market

- Validation, verification and IP qualification are major cost components of the design of any SoC
- Using pre-built IP-subsystems contributes to cost savings and faster time to market

Chip Design Costs

- Design: 30%
- Mask & Tooling: 40%
- IP Verification: 15%
- IP Qual & Validation: 15%

Customer IP

- AWE IP (PCIe/CXL, Ethernet, Memory I/F)
- Partner IP (CPU, Fabric, Security)
Future: Chiplets - “More-than-Moore” Solutions

**Smaller Disaggregated SOCs**
- **Scalable architecture**: adds dies to increase performance
- **Cost effective due to** better yields with smaller die
- **Reduced time to market by** combining custom SoC + available die

**Single System-on-Chip (SoC)**
- **Chip size limited to** maximum reticle size
- **Very large die typically with** lower yield and power limit
- **Bandwidth limited to** number of IO (data interconnect) on die
- **Time to market constrained by** design complexity and IP readiness

**Core SoC With IO Chiplets**
- **Higher Bandwidth enabled by** increased number of IO
- **Reduced time to market:**
  - Mix die from different nodes
  - Use pre-verified chiplets
- **Lower development cost** by sharing pre-built chiplets across products
Investments in Pre-built Chiplets

Targeted to the focused market segments

**IO Chiplet**
- Disaggregate Logic and IO
  - Integrated PCIe and Ethernet connected over D2D
  - Cost advantage to stay in N-1 node for IO chiplet

**Memory IO Chiplet**
- Memory Expansion
  - Expand DDR5 memory BW
  - Local cache with CPU

**Accelerator Chiplet**
- Co-processor/Accelerator
  - ARM/RISC-V high performance multi core
  - PCIe and DDRx connectivity

6 Chiplet Engagements
Custom Silicon – Ingredients for Success

Deep custom Silicon Expertise coupled with Connectivity IP Portfolio

- **Readily available, application optimized IP Sub-systems**
- **Proven design flow and methodology for leading nodes**
- **Experienced engineering teams and advanced (2.5D/3D) packaging expertise**
- **Reliable silicon operations with solid partnerships with manufacturing partners**
Flexible and Valued-Added Customer Engagement Model

Complete Spec-to-Silicon Capabilities
Custom Silicon Customer Engagement Phases

Leveraging Connectivity IP portfolio fuelling the design funnel

**Design & Pre-production Phase**
- **Product Development**
  - From 6 months to 2 years to provide prototypes
  - Driven by Non-recurring engineering (NREs)
  - From 6-24 months to provide initial prototypes
  - Typical NREs: $20m-$50m

**Post-production Phase**
- **Product life cycle 5-10 years**
  - From 3 to 6 months to fulfil POs
  - Driven by Unit price and volumes
  - Takes anywhere from 3-6 months to fulfil the POs
  - Product life cycle 5-10 years

10 major new design wins in 2022
20 tape-outs in 2022
14.5 million units shipped in 2022
Well Positioned to Grow

Value Proposition Enhanced Significantly With the Newly Integrated Teams

Focus on High growth market segments
Drive High value opportunities
Leverage IP portfolio to create differentiation
End-to-end expertise to deliver quality silicon
Drive larger and long tail revenue streams
Connectivity Products Group – A New Business Opportunity

Babak Samimi, Senior Vice President and General Manager Connectivity Products Group
Connectivity Products Group – A New Business Opportunity

- Alphawave is expanding its total solutions offering for the Data Center market
  - Growing from IP licensing to building the required companion connectivity SoC

- Uniquely positioned to leverage our IP portfolio to add a new growing business

- Untaps >$3B spend on opto-electronics semiconductors for connectivity
  - Dedicated SoC: connect rack-to-rack clusters and across data center campus networks

- Execution is underway, with initial products ramp in 2024
Growing Market Opportunity for Alphawave

1000x Volume Potential in Datacenter LAN (Intra) and WAN (DCI)

Datacenter LAN

Intra Connections

Datacenter WAN

MCN: Metro

Long-Haul

Reach
<10km
<100km
>100 to 1000s km

Device volume
10s millions
100s thousands
10s thousands
Connectivity Megatrends in Data Centers

**Big Data Growth + Processing Disaggregation Demand Unrelenting Innovation**

**Data Center LAN: CPU/Storage/AI**
Connection rates 100Gbps to 1.6Tbps

**Data Center WAN: Campus/DCI**
Connection rates 100Gbps to 800Gbps

**Big Data Signal Processing**
Signalling Complexity:
NRZ → PAM4 to Coherent

**Sustainability**
Reduce power per Gbps of connectivity

---

1 Data Center Interconnect

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Critical Technology & Innovations Required

Multi-Disciplined Architectural Expertise Required to Win

- Analog + Digital + Optics
- SoC + Chiplet
- PAM4
- Coherent
- System-on-Chip (SoC)
- High-Speed SerDes
- Programmable
- 112G to 224G
- Digital Signal Processing
- High-Precision Analog
- ADC / DAC
- >120G Baud

1 Analog to Digital Conversion / Digital to Analog Conversion
Alphawave Semi Has All The IP Required

IP Assets from Organic Investments and M&A

Anatomy of a Connectivity SoC Solution

SerDes: Serializer/Deserializer
Digital IP: Error Correction, Protocol Signalling
DSP: Digital Signal Processing
ADC: Analog to Digital Convertor
DAC: Digital to Analog Convertor
A Growing Addressable Market

First SoCs Going Into Production in 2024

Opto-Electronics Addressable Market

<table>
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<tr>
<th>Year</th>
<th>US$B</th>
</tr>
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<tbody>
<tr>
<td>2023</td>
<td>1.4</td>
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<td>2024</td>
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<tr>
<td>2025</td>
<td>3.6</td>
</tr>
<tr>
<td>2026</td>
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</tbody>
</table>

36% CAGR

Customer’s Big Data Processors

- Compute
- Storage
- AI/ML
- Switching

Lightcounting, company estimates
A New Business Opportunity

• Building on the foundations of our leading-edge capabilities and technologies

• Growth in Big Data and disaggregation of compute/storage processing will continue to demand complex innovations in opto-electronics connectivity solutions

• Industry is in the early innings of growth in PAM4 and Coherent adoption into data center networking – decadal investment cycle by the Hyperscalers

Anchored by the US$300m multi-year agreement with a leading North American hyperscaler, this business will significantly contribute to long-term revenue growth through the economic cycle.
Financial Overview

Daniel Aharoni, Chief Financial Officer
Strong Performance of Core IP Business

- **Cumulative Bookings (US$m)**
  - FY2019: 27
  - FY2020: 102
  - FY2021: 347
  - FY2022: >580

- **End Customers**
  - FY2019: 4
  - FY2020: 11
  - FY2021: 20
  - FY2022: 69

- **Pre-Tax Operating Cashflow (US$m)**
  - FY2019: nm
  - FY2020: 12
  - FY2021: 27

- **Backlog (US$m)**
  - FY2019: 16
  - FY2020: 37
  - FY2021: 169

- **Revenue (US$m)**
  - FY2019: 11
  - FY2020: 33
  - FY2021: 90

- **Adjusted EBITDA and Margin (US$m)**
  - FY2019: 3
  - FY2020: 19
  - FY2021: 52
  - Margin: 26% in FY2019, 59% in FY2020, 58% in FY2021

For definition of bookings, backlog and adjusted EBITDA see slide 94

1 As reported in Q4 2022 trading update. Includes customers from OpenFive who were not already customers of Alphawave and who signed contracts over from 1st September 2022. Revenue generating customers will be reported at FY 2022 results
Financial Roadmap

Oppunities for Growth

• Expanded TAM leveraging core IP with new routes to market
• Monetise core technology through IP Licensing and Silicon
• Coherent DSP technology for optical applications

Operational Efficiency

• Integrate and deliver on synergies from acquisitions
• Leverage expertise across enlarged group

Disciplined Capital Allocation

• Targeted investments in organic growth
• Optionality to pay down debt
Monetise Core IP Through Licensing and Silicon

Design Wins Lock in Long Tail of Royalties or Silicon Revenues

**Development Phase (c. 2 years)**
Revenue Recognised Over Development Period

**Production Phase (5-10 years)**
Revenues Recognised on Shipment

---

**LICENCE & NRE**
- Licensing
- NRE
- Support

**SILICON & ROYALTIES**
- Royalties
- Silicon

---

1 Includes IP, engineering, and masks & tooling
Revenue Trends

Increased Visibility to US$500m Revenue Run Rate in the Medium-Term

Development Phase (c. 2 years)
Revenue Recognised Over Development Period

- Typical pay-per-use IP licence US$5m-US$10m
- Multiple larger recurring revenue deals in pipeline
- Continuing momentum at 5nm and 3nm
- Acquisition synergies through bundled IP

Production Phase (5-10 years)
Revenues Recognised on Shipment

- First royalties paid in 2022
- Expected to contribute to earnings in 2023 and 2024

LICENCE & NRE

- Typical opportunity US$20m+
- Executing on acquired pipeline
- Leveraging our IP to target higher value opportunities

SILICON & ROYALTIES

- Executing on acquired backlog of over US$150m
- Long-tail of silicon revenues
- Strategic focus on high-end silicon opportunities

- New business opportunity
- Self-funded - no revenues during development phase

1 Estimate, subject to purchase price accounting and acquisition accounting adjustments

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Headcount Increase Driven by M&A and Organic Recruitment

Technology Led Organisation – 90% Employees in R&D / Engineering

Number of Employees

<table>
<thead>
<tr>
<th></th>
<th>Q4 2021</th>
<th>Q1 2022</th>
<th>Q2 2022</th>
<th>Q3 2022</th>
<th>Q4 2022</th>
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<th>Q3 2023E</th>
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<td>181</td>
<td>235</td>
<td>617</td>
<td>695</td>
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</table>

By Function

- R&D: 90%
- G&A: 8%
- S&M: 2%

By Region

- Canada: 37%
- USA: 43%
- India: 9%
- Israel: 7%
- China: 3%
- Taiwan: 2%
- UK: 1%

Due to rounding, percentages may not precisely reflect the absolute figures

- Focus on critical hires to support growth opportunities
- Targeting <10% headcount growth in 2023

Main Locations
Strong Focus on Operational Efficiency

Targeting 30% Medium-Term Opex % of Revenue

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<thead>
<tr>
<th>Closing Headcount</th>
<th>2020</th>
<th>2021</th>
<th>H1 2022</th>
<th>FY 2022</th>
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<td>204</td>
<td>621</td>
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<td>S&amp;M</td>
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<td>G&amp;A</td>
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<td>Permanent</td>
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<tr>
<td>Interns</td>
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<td>5</td>
<td>16</td>
<td>47</td>
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</table>

Operating expenses include depreciation and exclude IPO-related expenses, one-time M&A related expenses, share-based payments and FX gains and losses.
Disciplined Capital Allocation

Targeted Capital Deployment Over the Next Two Years

**Organic Growth**
- Focus on critical hires/expertise to support growth opportunities
- Investment in own product development and prototyping

**Debt Repayment**
- Optionality to pay down debt with cash on hand
- Strategy driven by USD/GBP exchange rates and interest rates

**M&A**
- No significant M&A planned
2023 Guidance Post-Banias

Revenues\(^1\) (US$m)

- Lower end of revenue guidance increased given strong performance in Custom Silicon and early realization of synergies
- Banias acquisition not expected to generate revenues until 2024

Adjusted EBITDA\(^{1,2}\) (US$m) and Margin

- Tail of profitable but lower margin custom silicon revenues acquired
- Product R&D investment expected to be partially capitalised under IAS38 given commercial and technical feasibility

\(^1\) Charts not drawn to scale
\(^2\) For the definition of adjusted EBITDA see slide 94
\(^3\) At the mid-point of the guidance range, assuming 25% adjusted EBITDA margin

1 $210m-$240m
2 $180m-$210m
3 $340m-$360m

50% - 60%
Mid-forties %
32% - 36%

Approx. $87m\(^3\)
Medium-Term Operating Model

<table>
<thead>
<tr>
<th>US$</th>
<th>2023</th>
<th>2025</th>
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<tr>
<td>Revenues</td>
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<td>Gross margin</td>
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<td>Opex %</td>
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<tr>
<td>R&amp;D %</td>
<td>Below 20%</td>
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| Adjusted EBITDA¹ | Approx. $87m  | Approx. $150m |
| Adjusted EBITDA % | c. 25%      | c. 30%       |
| Capex (exc. Cap R&D) | c. 12%      | c. 10%       |

- 2023-2025 revenue CAGR of approximately 20%
- Operating expenses as a percentage of revenue gradually decreasing towards 30%
- Adjusted EBITDA growing faster than revenue over the period resulting in 5% improvement in adjusted EBITDA margin
- Capex increase driven by investment in own products

¹ 2023 assumes mid-point of the guidance range and 25% adjusted EBITDA margin; 2025 assumes US$500m revenue and 30% adjusted EBITDA margin
Key Takeaways

• Capital deployment in 2022 accelerated our transition to a vertically integrated business

• Creates significant further opportunities for growth and TAM expansion

• Continued disciplined financial management and increased operating efficiency

• Capital allocation focused on debt paydown and targeted organic investment
QA Session
Greater Scale of Vertically Integrated Model

Delivering Accelerated Revenue Growth

- High-growth expanded addressable market accessible by vertically integrated business
- Wider offering of connectivity silicon IP, custom silicon and opto-electronic products focused on data centers and wireless infrastructure
- Supports our long-term ambition of $1 billion revenue run rate by 2027

Addressable Market $B

- 2023 Revenue $340-$360m
- Market growth supports long-term growth target

- Monetise IP through licence, custom silicon and connectivity products
- Enhanced competitive position and greater scale
Thank You!
References Slides 15 and 32

- **Streaming Services** [Video Streaming (SVoD) - Global | Statista Market Forecast](https://www.statista.com/statistics/1183457/streaming-video/) Revenue is expected to show an annual growth rate (CAGR 2022-2027) of 11.48%, resulting in a projected market volume of US$139.2bn by 2027

- **Social Media Users** [Number of worldwide social network users 2027 | Statista](https://www.statista.com/statistics/1183457/social-media-users-number-worldwide/) Number of users from 4.26 billion in 2021 to almost six by 2027

- **VR/AR** [IDC Spending Guide Forecasts Strong Growth for Augmented and Virtual Reality](https://www.idc.com) The five-year compound annual growth rate (CAGR) for AR/VR spending will be 32.3%. Virtual reality will account for more than 70% of all AR/VR spending throughout the 2022-2026 forecast

- **Cloud Services** [Gartner Forecasts Worldwide Public Cloud End-User Spending to Reach Nearly $500 Billion in 2022](https://www.gartner.com) 2021:$419m 2023 $600m

- **AI** [IDC Forecasts 18.6% Compound Annual Growth for the Artificial Intelligence Market in 2022-2026](https://www.idc.com)


- **e-commerce** [Global Ecommerce Growth Forecast 2022 | Morgan Stanley](https://www.morganstanley.com) Over the long term, the e-commerce market has plenty of room to grow and could increase from $3.3 trillion today to $5.4 trillion in 2026.

- **5G Services Market** [Global 5G Services Market Size is Anticipated to Reach (globenewswire.com)](https://www.globenewswire.com) The global size to grow from USD 53.0 billion in 2020 to USD 249.2 billion by 2026, at a Compound Annual Growth Rate (CAGR) of 29.4% during the forecast period.
Non-GAAP Metrics


- Bookings are a non-IFRS measure representing legally binding and largely non-cancellable commitments by customers to license our technology. Bookings comprise licence fees, non-recurring engineering, support and, in some instances, our estimate of potential future royalties.

- Backlog is a non-IFRS measure representing our bookings less revenues recognised to date.

- Adjusted EBITDA excludes IPO-related non-recurring costs, foreign exchange adjustments, share-based payments, M&A-related expenses and one-time legal fees associated with WiseWave.