



The Role of Connectivity Technology in AI

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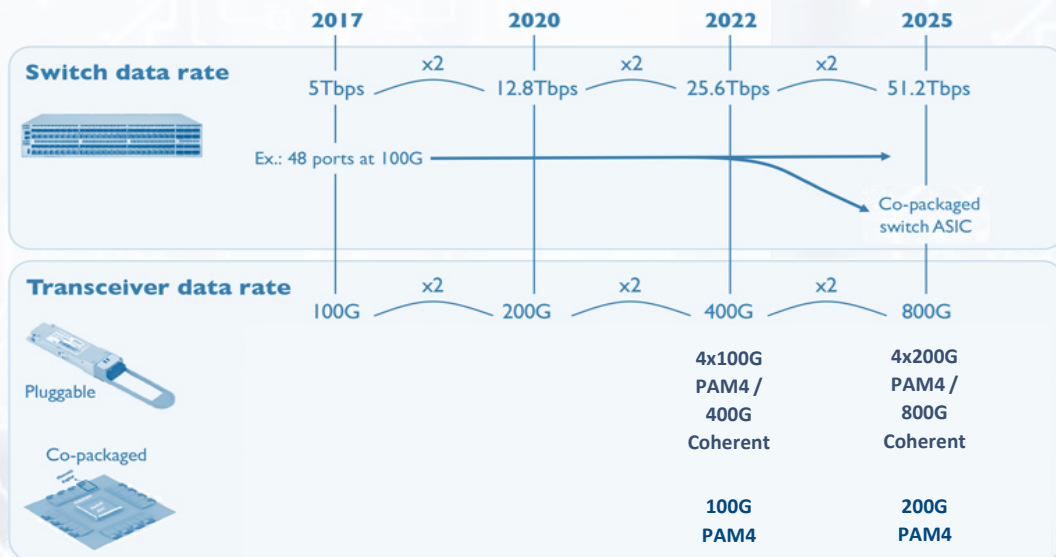
Agenda

- The Role of Connectivity Technology and AI
- The Impact of AI on...
 - Networks
 - Processors
- Q & A



Artificial Intelligence - Connectivity Is Its Life Blood

Data Rates Double every 2-3 Years



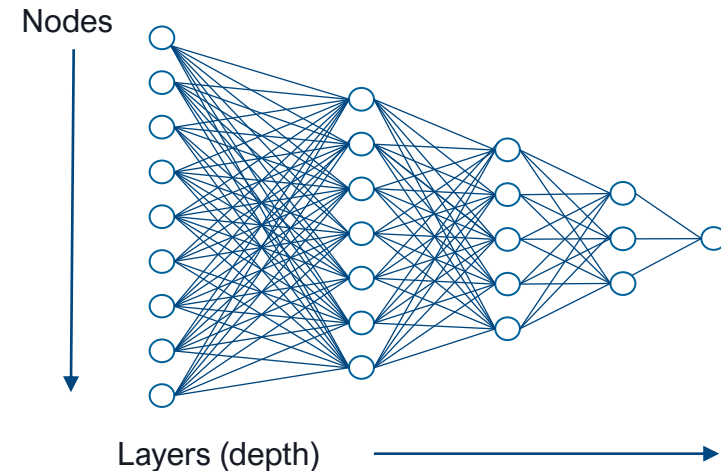
- AI/ML technologies require huge amounts of data
- **Data bandwidth and latency for connections within the datacentre become essential** and hyperscalers are making the necessary investments so as not to limit the potential of AI
- Thousands of components, wires, switches, ports, and more are organized in data centers to connect everything together

Source: "Silicon Photonics Market and Technology Report 2020", April 2020
Silicon Photonics Market & Technology 2020 - Yole Développement (i-micronews.com)

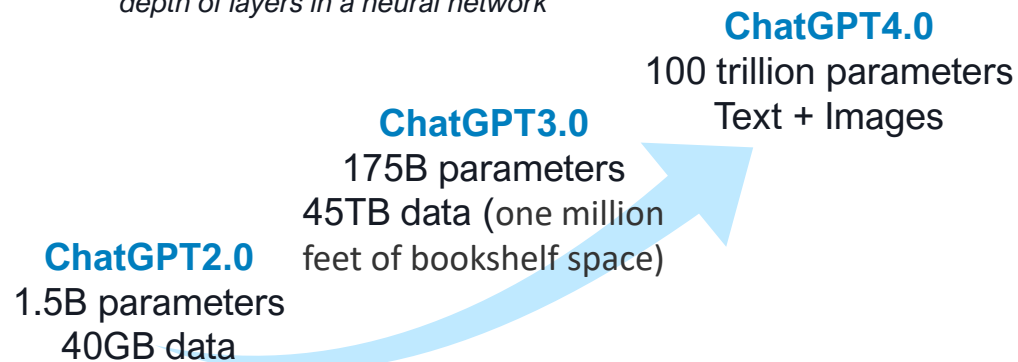


Deeper Neural Networks Using Vast Amounts of Data

Imposing Different Requirements in The Digital Infrastructure



The “deep” in deep learning refers to the depth of layers in a neural network



- Neural networks are a series of algorithms that mimic the operations of a brain to recognize relationships between vast amounts of data
- Nodes perform similar computations on their inputs ⇒ Tremendous parallelism is possible
- Neural networks rely on training data to learn and improve their accuracy over time
- To understand better the requirements imposed in the digital infrastructure we need to understand the two types of AI compute workloads



AI Compute Workloads – Training and Inference



Training workloads process huge amounts of data

- More training data makes it more accurate and more useful
- Training hardware processes vast data very quickly, requiring high bandwidth density



Inference workloads perform tasks in real-time

- AI models perform useful tasks for multiple users at the same time (i.e. image recognition or autonomous driving)
- Low-latency connectivity is critical

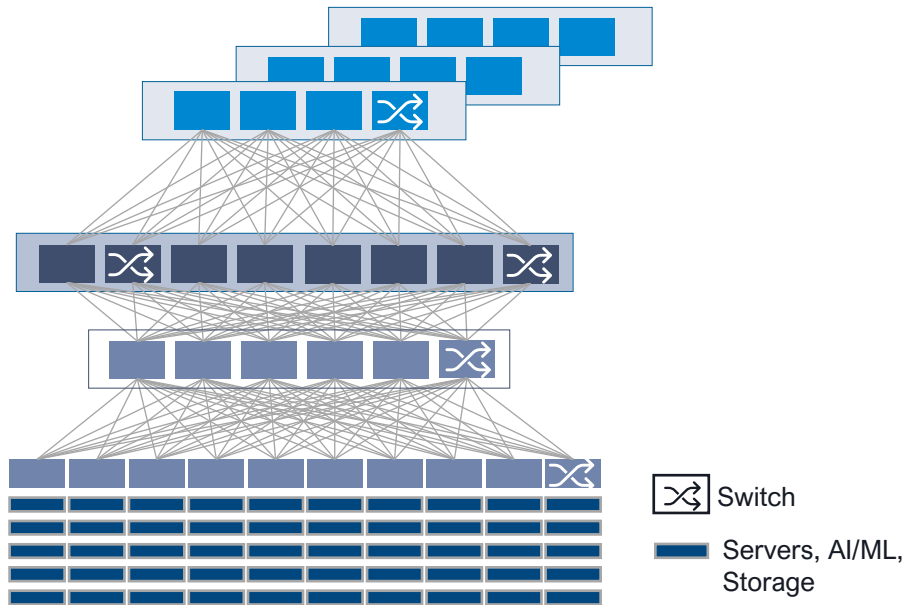
Low-power, High-bandwidth Connectivity Required Throughout



The Impact of AI

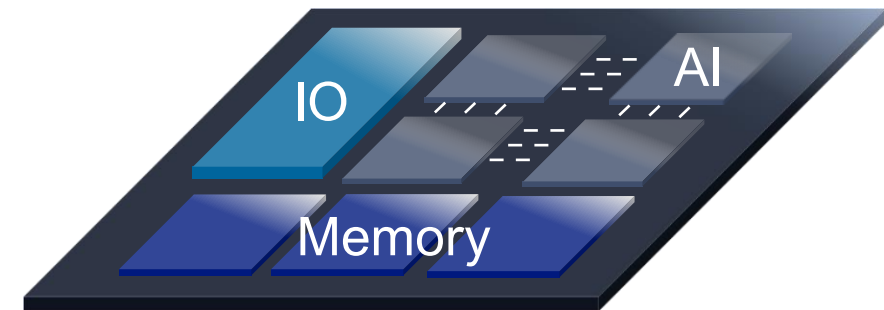
... on the Network

- AI is driving increased bandwidth demands throughout the network for training and inference



... on the Processors

- Trend towards purpose-built processors for AI training/inference with high connectivity demands



IO – Input/Output – Data connectivity



The Impact of AI

... on the Network

Increasing Connectivity Demands

Higher data rates, lower cost, power and latency

Disaggregated Computing

Disaggregation of compute and storage to increase efficiency

... on the Processors

CMOS Technology Scaling

Advanced technologies deliver massive processing power with higher development and manufacturing costs

Chiplet

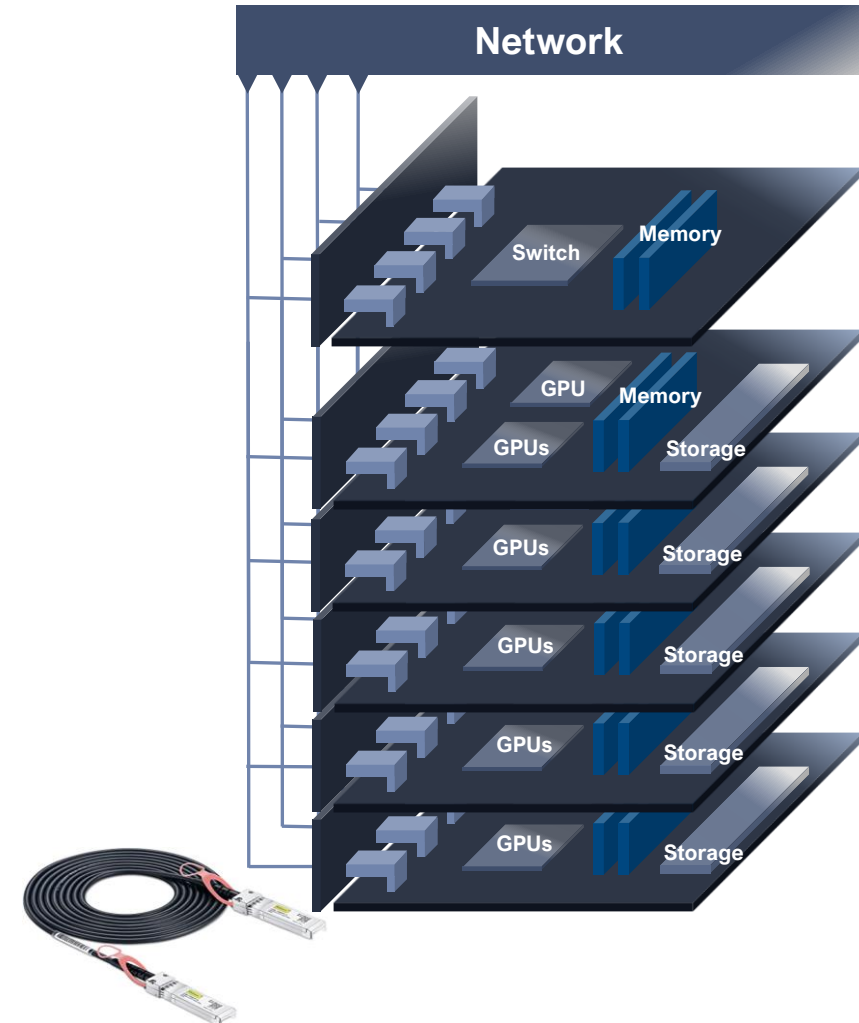
Emergence of the chiplet design paradigm



Increased Connectivity Demands for AI

Alphawave Technologies For Both Copper and Optical Connectivity

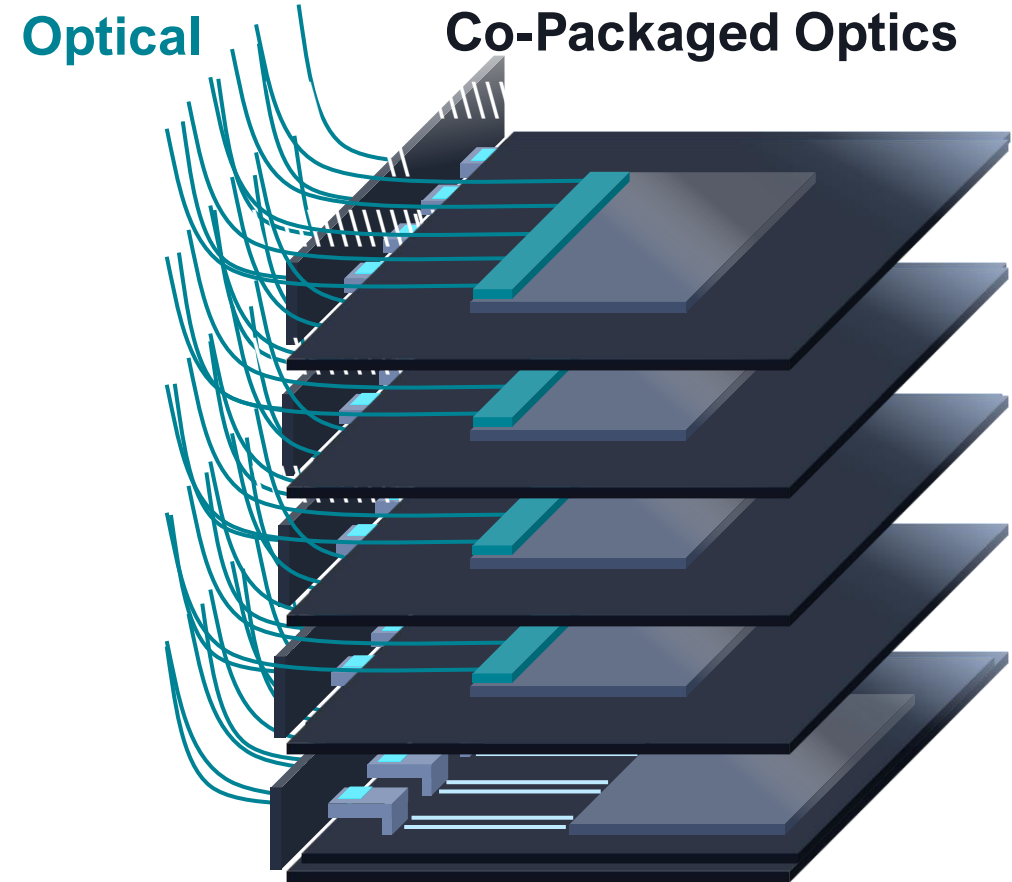
- Copper wiring establishes high-speed connections on each circuit board
- Cables connect processors in racks to each other, today mostly copper cables
- Aggregated data traffic flows across longer distances up to a few kilometres
- To process more data in larger neural networks, more parallel hardware is added
- High-performance connectivity IP maintains signal integrity in challenging applications
- Connectivity products are required to deliver more bandwidth across the networks



Trends Towards Optical Connectivity

Alphawave Technologies For Both Copper and Optical Connectivity

- Future AI clusters will be larger and interconnected with optics
- Emerging trend towards co-packaged optics eliminates intervening receivers and re-transmitters
- Alphawave is well positioned to benefit from these trends. Our solutions' reach and robustness eliminate the need for additional re-transmitters.



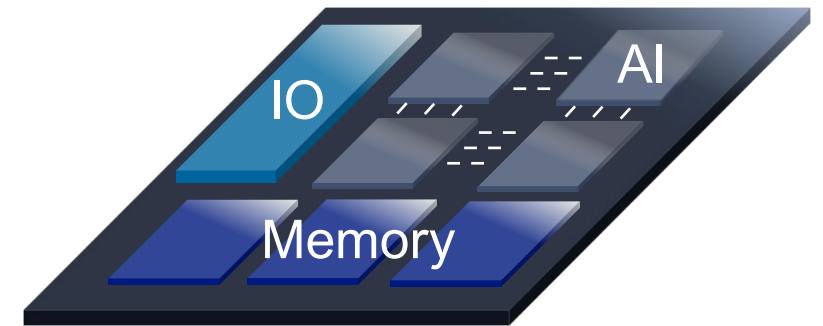
Additional re-transmitters —



Chiplet Processor Architectures Rely on Connectivity

Alphawave is at The Forefront of The New Chiplet Design Paradigm

- Chiplets are individual dies that are co-packaged side-by-side. The combination operates and is sold as a single chip
- Enable processor chips larger than is possible on a single die
- Smaller dies allow for higher yield, lowering the cost of manufacturing
- Reduce time to market by being able to mix and match pre-validated chiplets with different functionalities to create new systems (custom configuration)
- Relies on a fabric of dense high-speed interconnect: UCIe¹, HBM
- IO chiplets provide connectivity beyond the package



IO – Input/Output – Data connectivity



¹ <https://www.uciexpress.org/>

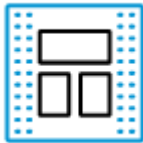
Our Technology Supports AI Connectivity Requirements



Low-Power High-Bandwidth Connectivity Required

- Disaggregation to increase efficiency
- Increasing demand for higher data rates, low cost, low power and latency

**Connectivity
Products for Both
Copper and Optical
Cables**



Purpose-Built Processors With High Connectivity Demands

- Emergence of chiplet processor architectures
- Smaller dies enable lower manufacturing costs

**At the Forefront of
Chiplet Design**





QA



Thank You!