ALPHAWAVE SEMI

Advanced Custom Silicon For AI and Data Center

Mohit Gupta, Senior Vice President and GM Custom Silicon and IP

21 March 2024

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Certain statements included herein may constitute forward-looking statements within the meaning of the securities laws of certain jurisdictions. Certain such forward-looking statements can be identified by the use of forward-looking terminology such as “believes”, “expects”, “may”, “are expected to”, “intends”, “will”, “will continue”, “should”, “would be”, “seeks”, “anticipates” or similar expressions or the negative thereof or other variations thereof or comparable terminology. These forward-looking statements include all matters that are not historical facts. They include statements regarding Alphawave IP Group Plc’s (”Alphawave IP”) intentions, beliefs or current expectations concerning, amongst other things, its results in relation to operations, financial condition, prospects, growth, strategies and the industry in which it operates. By their nature, forward-looking statements involve risks and uncertainties because they relate to events and depend on circumstances that may or may not occur in the future. Forward-looking statements are not guarantees of future performance and Alphawave IP’s actual results of operations, financial condition, and the development of the industry in which it operates, may differ materially from those made in or suggested by the forward-looking statements contained in this Presentation. In addition, even if Alphawave IP’s results of operations, financial condition, or the development of the industry in which it operates are consistent with the forward-looking statements contained in this Presentation, those results or developments may not be indicative of results or developments in subsequent periods. Important factors that could cause those differences include, but are not limited to customer demand, Alphawave IP’s innovation and R&D and technology capabilities, target market trends, industry trends, customer activities and end-market trends, market acceptance of Group technologies; increased competition; macroeconomic conditions; changes in laws, regulations or regulatory policies; and timing and success of strategic actions. These forward-looking statements speak only as of the date of this Presentation. As such, undue reliance should not be placed on forward-looking statements. Other than in accordance with legal and regulatory obligations, Alphawave IP undertakes no obligation to publicly update or revise any forward-looking statement, whether as a result of new information, future events or otherwise.

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Bringing Customer Ideas to Life in Specialized Silicon

Mohit Gupta, Senior Vice President and General Manager Custom Silicon and IP

Agenda

- AI and the era of specialized silicon
- Our strategy
- Success stories
- Custom SoC business model
- Summary

Rise of Custom Silicon and Chiplets in Data Centers

PERFORMANCE

UPTO 4 CHIPLETS
350W
DDR5, HBM2E
PCIe5/CXL

INTEL XEON
Sapphire
Rapids

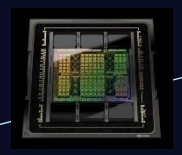
UPTO 13 CHIPLETS
200-400W
DDR5
PCIe5/CXL

AMD EPYC
4th Gen
Genoa

MONOLITHIC GPU
700W
80B Transistors
814mm2

80GB HBM3
3TB/S Memory BW
900GB/S NV-Link4

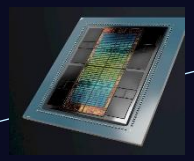
NVIDIA
H100



12 CHIPLETS
700W
153B Transistors

192GB HBM3
5.2TB/S Memory BW
896GB/S Infinity Fabric BW

AMD
MI300X



CPU
General Purpose
@ lower performance

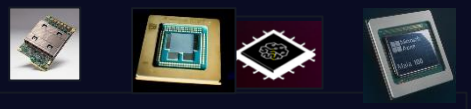
GPU
Domain specific language
(eg. CUDA)

Google aws Microsoft

TPU4, TPU5

Graviton3
Trainium

Maia 100



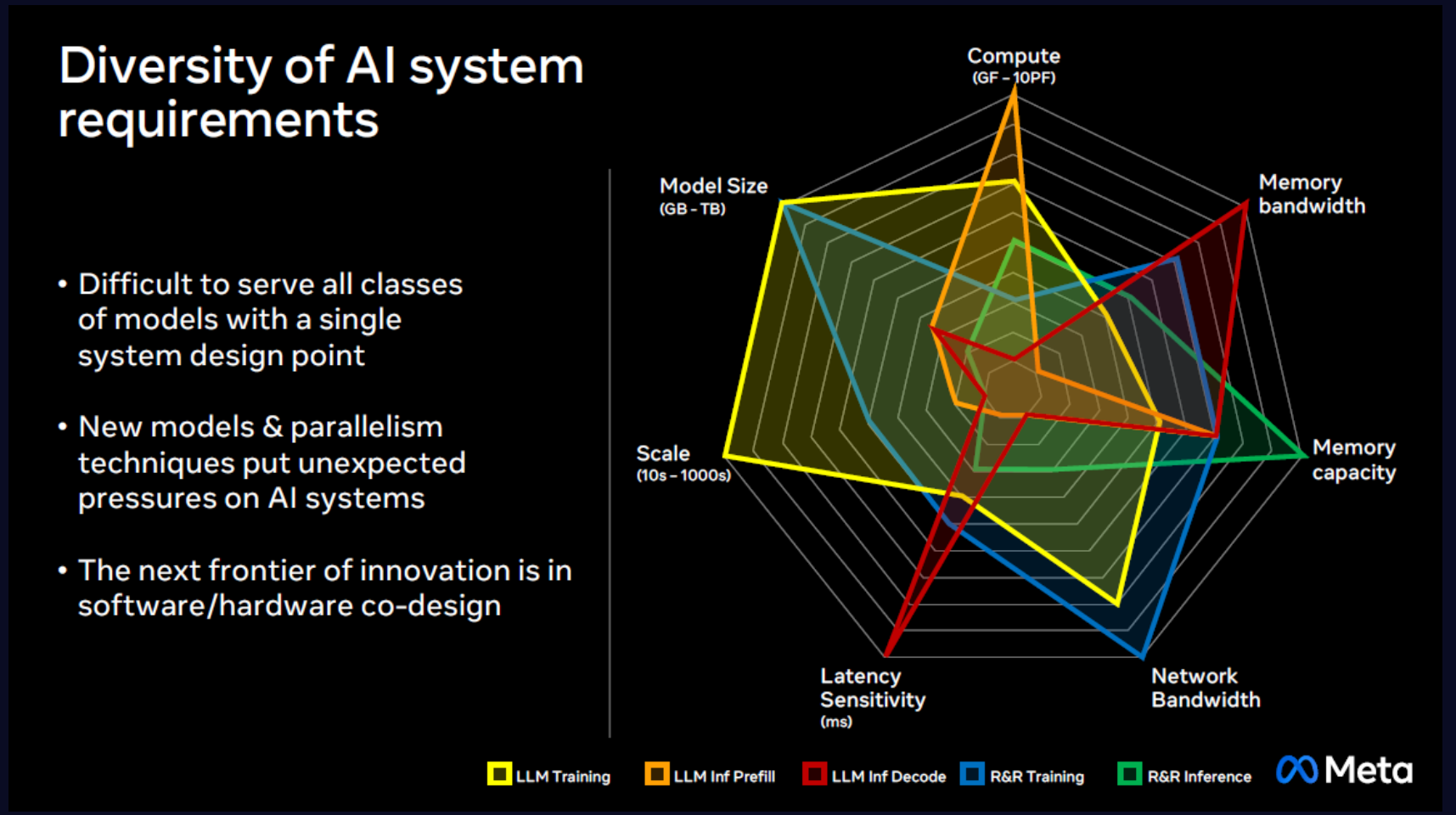
CUSTOM SILICON
Optimized for AI

2010 → 2017 → 2020 → TIME

Time: Denotes approximate introduction of first product in the category

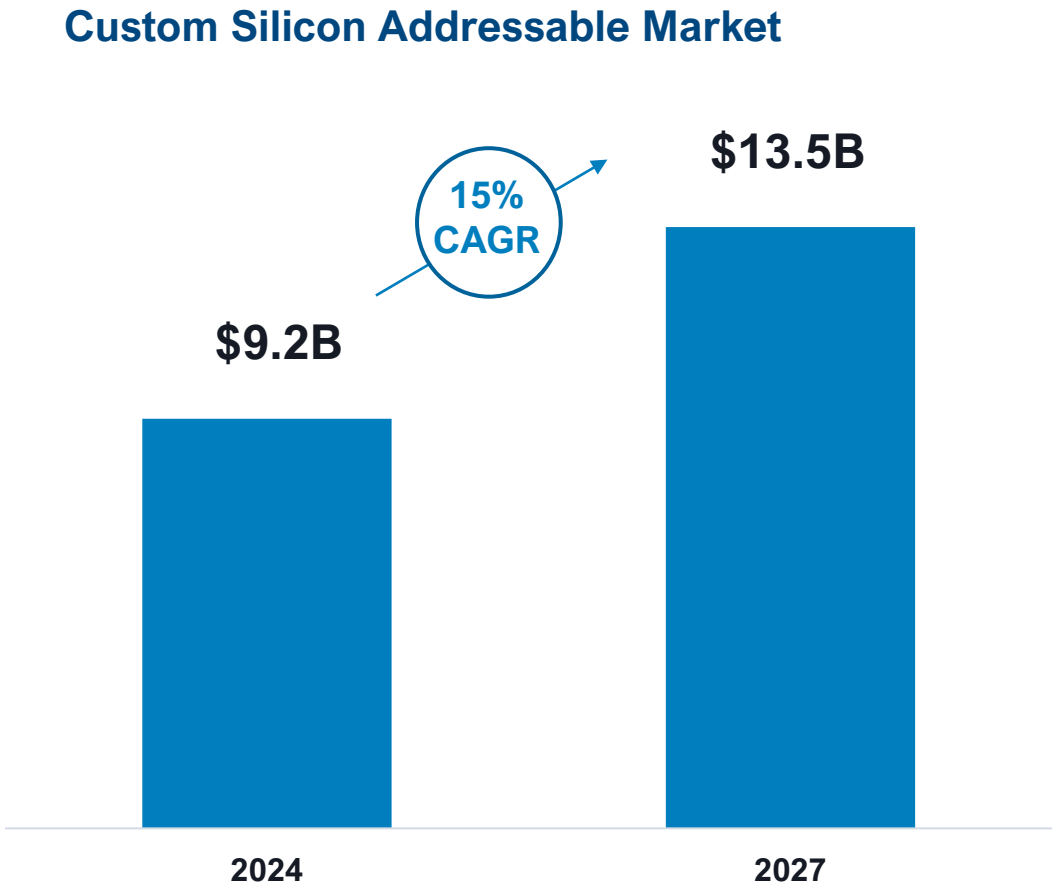
AI Workload Diversity

“Open Infrastructure Platforms to usher in age of GenAI”



Source AI Summit : “Leading with Open” Meta

A Growing Addressable Market



Semico Research Corporation, November, 2023

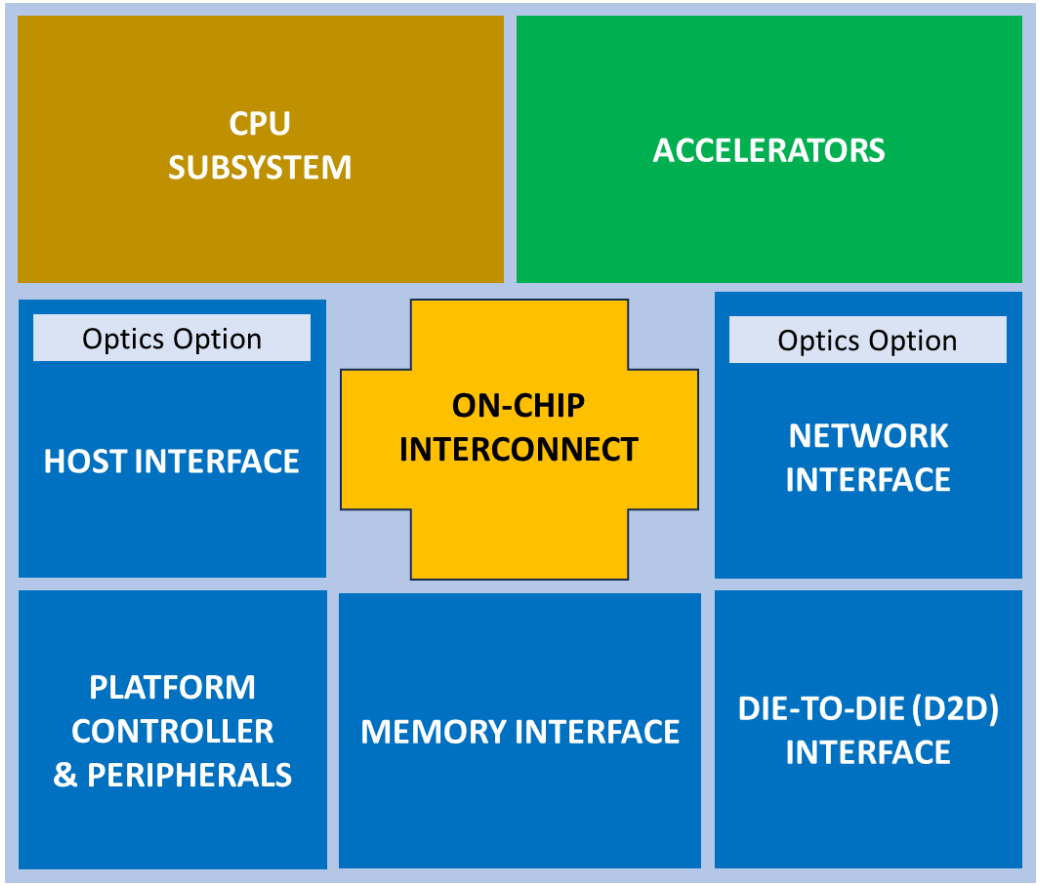
Maximizing Performance With Optimized Power For Specific Use Cases

- Purpose-built custom SoCs leveraging high-speed connectivity with increasing levels of compute
- Targeted at high-end, data center infrastructure market segments

- Optimized to specific use cases
  - AI LLM training and inference acceleration, video streaming servers, accelerators for public cloud, etc

Introducing the Composable SoC for Data Centers

Faster time-to-market through silicon-proven IP blocks combined with customer-specific accelerator IP



CONNECTIVITY

+

COMPUTE

+

ACCELERATION

+

ADVANCED PACKAGING & PROCESS NODES

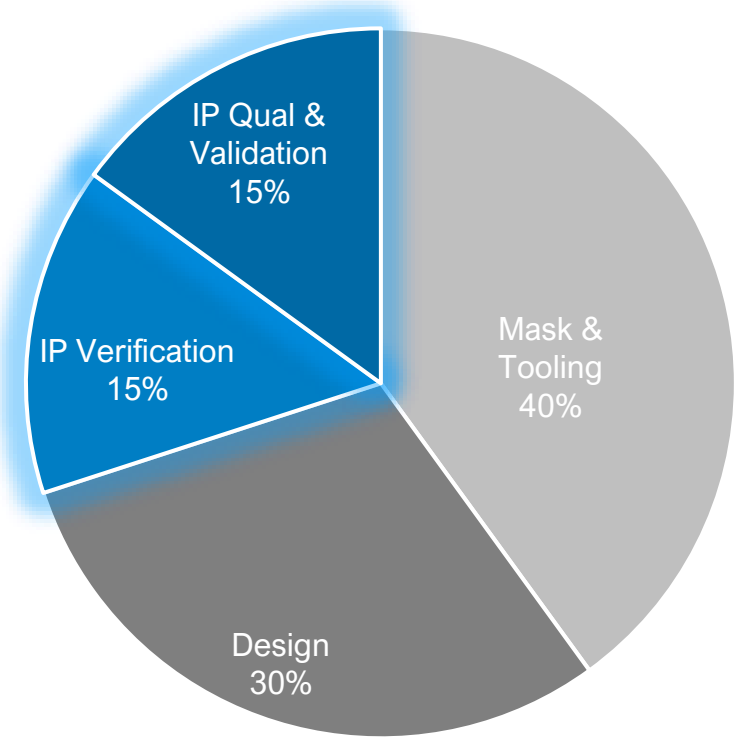
=

Faster Time-to-Market, Cost-Effective, Power-Efficient Custom Silicon Solutions

Benefits of Pre-Built “Application Optimized” IP Subsystems

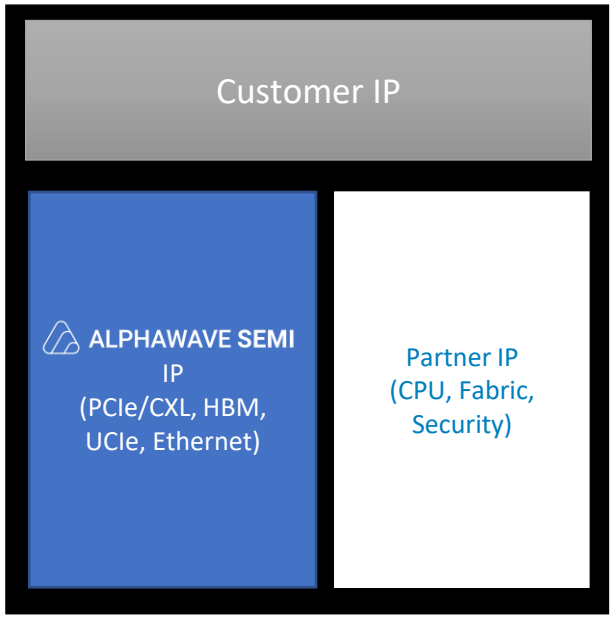
Lower Costs and Faster Time to Market

Chip Design Costs



Source: IBS, July 2022

- Validation, verification and IP qualification are major cost components of the design of any SoC
- Using pre-built IP-subsystems contributes to cost savings and faster time to market



Full Portfolio of High-Performance Connectivity Silicon IP

COMPUTE
PCIe / CXL

High-speed Interface IP for data centre compute – CPU, GPU, AI & FPGA

PCIe GEN6 / CXL 3.0

NETWORKING
ETHERNET

112Gbps & 224Gbps PAM4 Interface IP for Networks – Switches, Routers, DPUs, NICs

400G, 800G, 1.6T ETHERNET

MEMORY
HBM

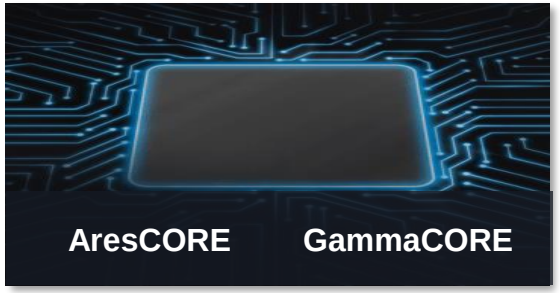
Memory Interface IP for HBM - CPU, GPU, AI, FPGA, DPUs

HBM3 AND HBM4

CHIPLETS
UCIe

Chiplet Interface IP 2.5D and 3DIC

UCIe, STREAMING, CHI/CXS



Leading the Way for Chiplets

Silicon-proven 3nm Universal Chiplet Interconnect Express™ (UCIe™) Subsystem

Low power, low latency, flexible and complete die-to-die (D2D) solution

- 24Gbps data-rate-per-lane
- Architecture is compliant with the latest UCIe Specification Revision 1.1
- Supports
  - x16 or x32 Standard Package
  - x32 or x64 Advanced Package

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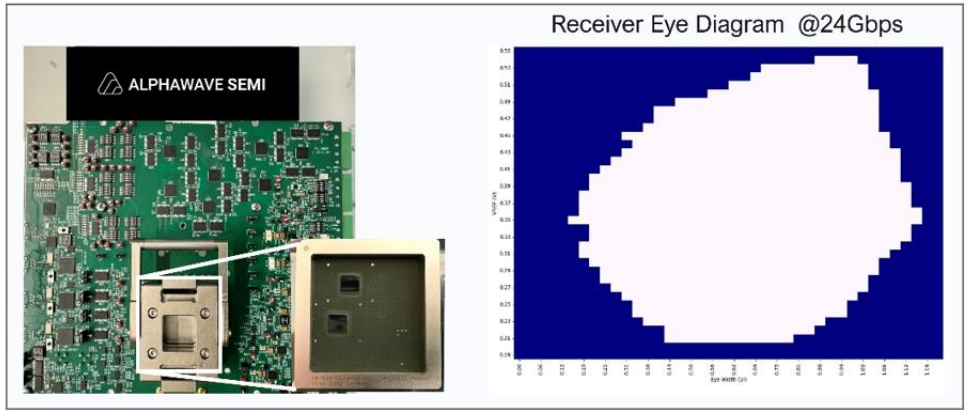
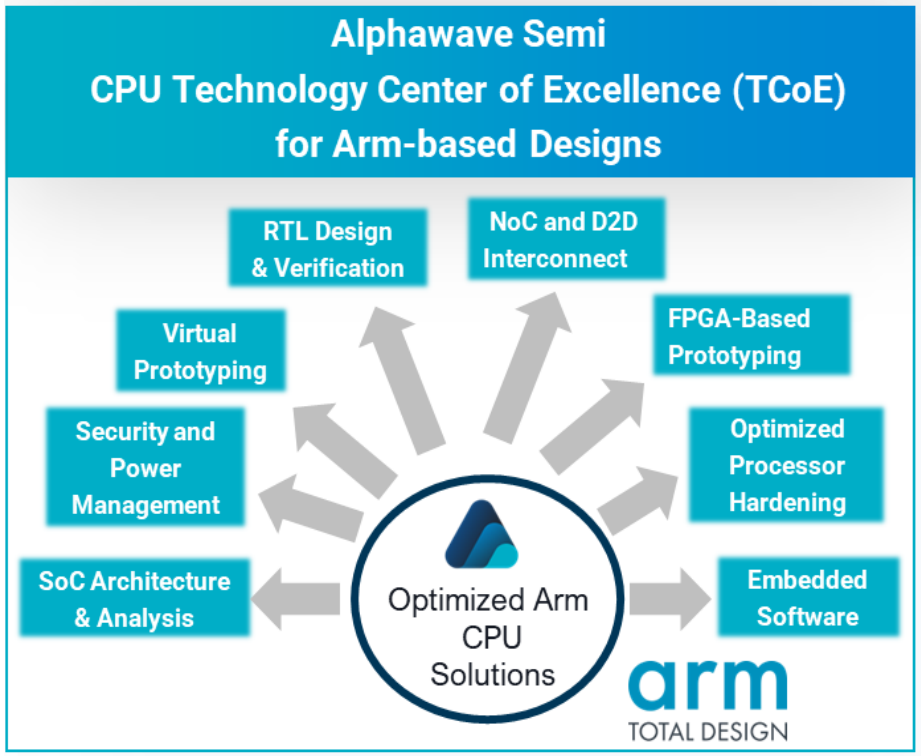
Alphawave Semi Demonstrates 3nm Silicon-Proven 24Gbps Universal Chiplet Express™ (UCIe™) Subsystem for High-Performance AI Infrastructure

Successful silicon bring-up extends leadership in chiplet-enabled silicon solutions to accelerate AI connectivity and compute



Alphawave Semi 24Gbps UCIe 3nm silicon platform

High Performance Compute Subsystems Through Arm Total Design



- Alphawave Semi joined as a founding IP and Custom Silicon member
- Provides accelerated path for specialized SoC solutions based on Arm Neoverse Compute Subsystems (CSS)
- Multiple Arm cores in production optimized for performance, power and area (PPA)
- Our connectivity IP seamlessly complements Arm IP
  - Supports Arm fabric interfaces such as AXI and CHI/CXS
  - Enables easy integration of advanced connectivity such as PCIe/CXL™, HBMx, DDRx, Ethernet and UCIe

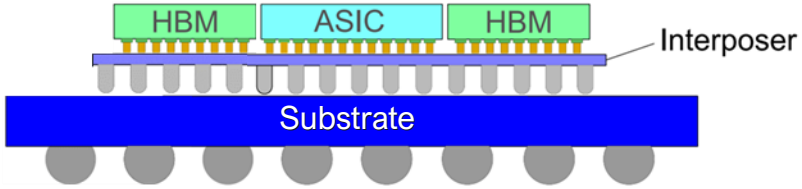
Leading-Edge SoCs and Chiplets in Advanced Packaging

Complex High-Performance SoCs

- High bandwidth with scalable architecture
- Many multi-GHz Arm CPU cores
- Complex 2.5D Packaging

Implementation example: HPC Customer SoC

Large Die: > 600 mm2
4 x HBM
2.5D CoWos Package
70mmx70mm, 5000+ balls



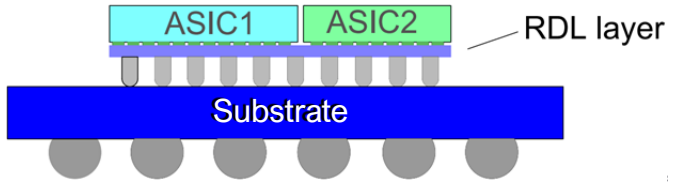
Chiplets: I/O | Memory | Compute | Accelerator

- High bandwidth with scalable architecture
- UCIe enabled
- 2.5D InFO_oS packaging

Implementation example: AI Accelerator Chiplet

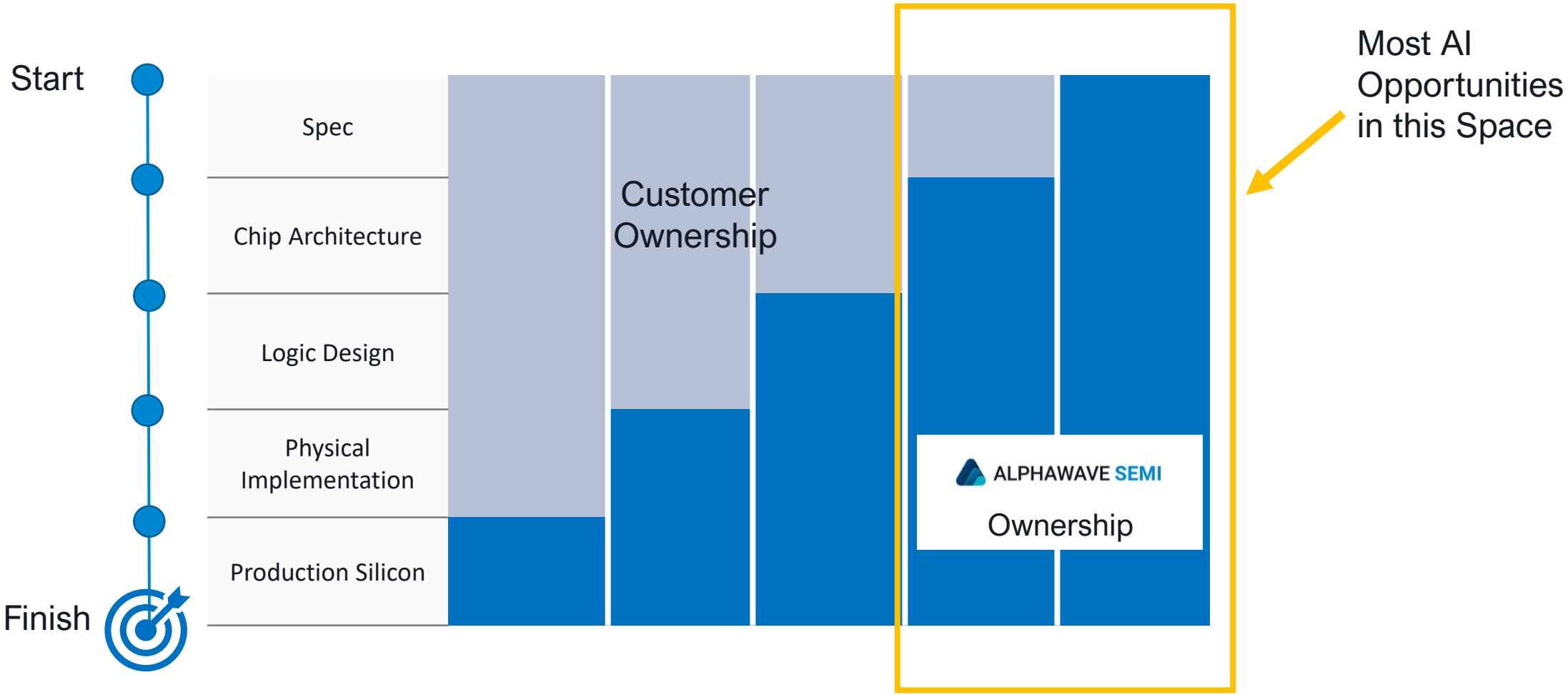
Early InFO-oS tape-out at TSMC

5 RDL layers interconnecting two dice

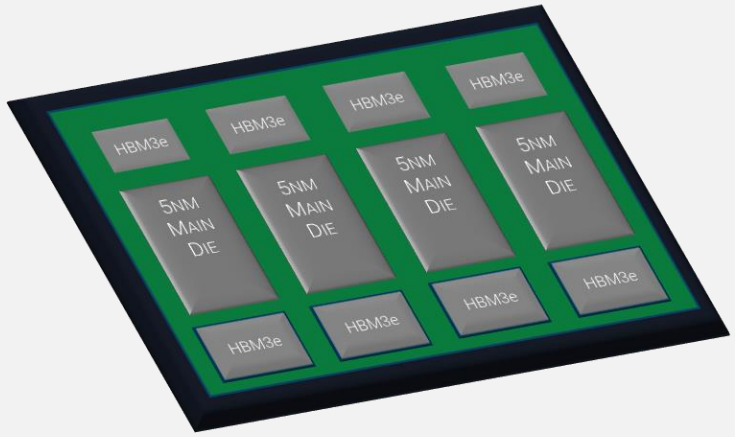


Flexible and Valued-Added Customer Engagement Model

Complete Spec-to-Silicon Capabilities



Early Success Driven by Leading IP Portfolio

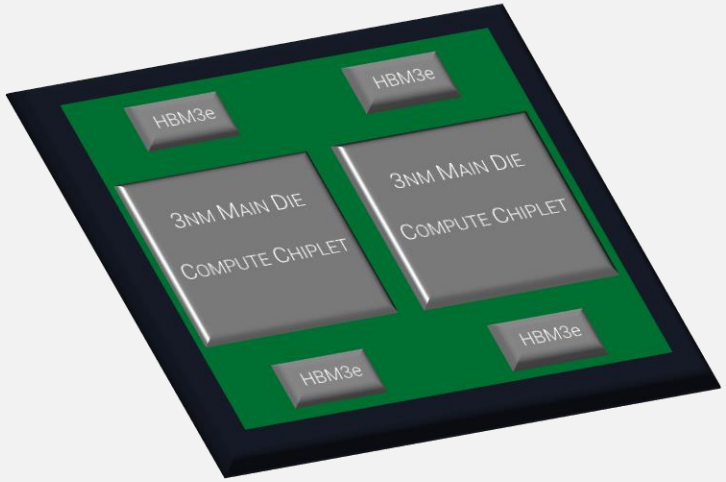


5NM AI ACCELERATOR CHIP

Customer Provided Accelerator IP

UCIe/PCIe/Ethernet/HBM3e subsystems

4x Main Dies + 8 HBM3e : ~ 60mm x 80mm

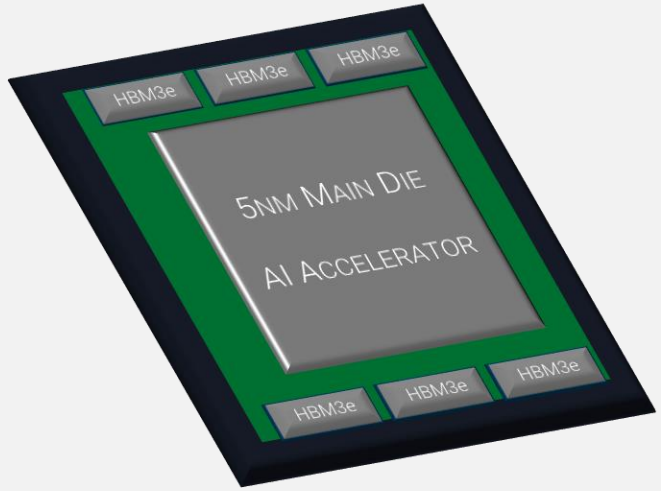


3NM ARM NEOVERSE BASED HPC CHIP

Arm Compute Subsystem

HBM3e/DDR/PCIe/UCIe Subsystems

2x Main Dies + 4 HBM3e: ~ 70mm x 70mm



5NM AI ACCELERATOR CHIP

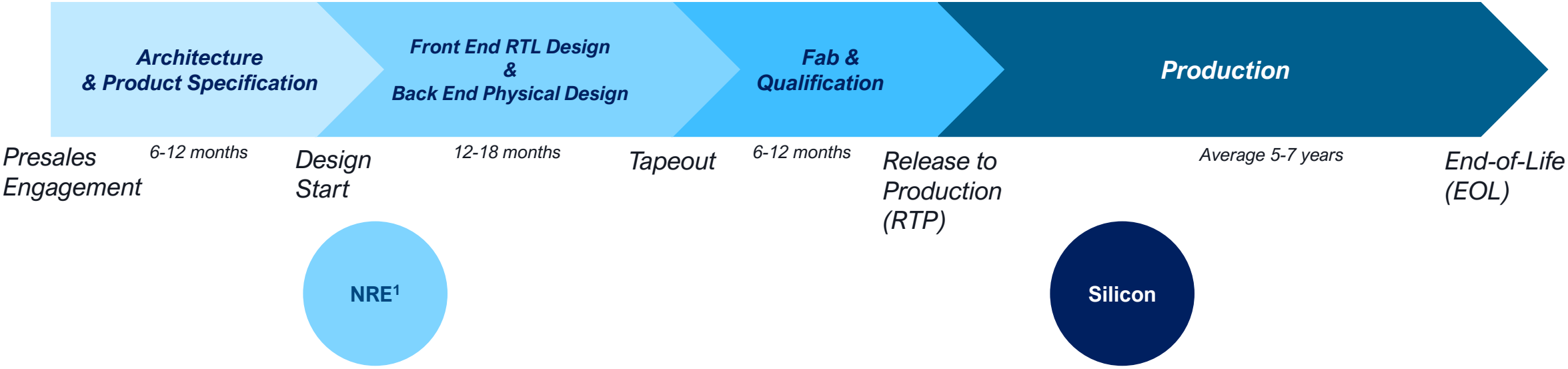
Power-packed Reticle size chip (>800 sqmm)

HBM3e/112G/PCIe Subsystem

1x Main Die + 6 HBM3e: ~ 70mm x 70mm

Custom Silicon Revenue Profile

Design Wins Start with NRE and Lock in Long Tail of Silicon Revenues



Reported in Licence & NRE
Revenue Recognised Over Development Period

Reported in Silicon & Royalties
Revenue Recognised on Shipment

[1] Includes IP, engineering, and masks & tooling

Summary

- Generative AI driving the need for specialized silicon to meet performance requirements while optimizing power
- Our Composable SoC and chiplets approach leverages proven connectivity IP subsystems and Arm Total Design compute for faster time-to-market
- Leading edge offering built on a full set of leading IP, custom silicon design expertise, advanced packaging and silicon operations
- Custom Silicon has a 3 to 10+ year revenue profile from initial engagement

QA Session

Thank You!