Welcome

Jose Cano, Global Head of IR

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Agenda

Welcome	Jose Cano, Global Head of IR
The Next Leader of Connectivity for AI	Tony Pialis, Co-Founder and CEO
AI and Data Centre Megatrends	Tony Chan Carusone, CTO
Silicon IP	Jonathan Rogers, Co-Founder and SVP Engineering
Path to Billions	Charlie Roach, Chief Revenue Officer
Break	
IP, Chiplets and Custom Silicon	Mohit Gupta, SVP & GM Custom Silicon and IP
Connectivity Products – Multi-Billion Dollar Market	Babak Samimi, SVP & GM Connectivity Products
Financial Overview	Rahul Mathur, Chief Financial Officer
Closing Remarks	Tony Pialis, Co-Founder and CEO
QA Session	Executive team

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Safe Harbour

Certain statements included herein may constitute forward-looking statements within the meaning of the securities laws of certain jurisdictions. Certain such forward-looking statements can be identified by the use of forward-looking terminology such as “believes”, “expects”, “may”, “are expected to”, “intends”, “will”, “will continue”, “should”, “would be”, “seeks”, “anticipates” or similar expressions or the negative thereof or other variations thereof or comparable terminology. These forward-looking statements include all matters that are not historical facts. They include statements regarding Alphawave IP Group Plc’s (”Alphawave IP”) intentions, beliefs or current expectations concerning, amongst other things, its results in relation to operations, financial condition, prospects, growth, strategies and the industry in which it operates. By their nature, forward-looking statements involve risks and uncertainties because they relate to events and depend on circumstances that may or may not occur in the future. Forward-looking statements are not guarantees of future performance and Alphawave IP’s actual results of operations, financial condition, and the development of the industry in which it operates, may differ materially from those made in or suggested by the forward-looking statements contained in this Presentation. In addition, even if Alphawave IP’s results of operations, financial condition, or the development of the industry in which it operates are consistent with the forward-looking statements contained in this Presentation, those results or developments may not be indicative of results or developments in subsequent periods. Important factors that could cause those differences include, but are not limited to customer demand, Alphawave IP’s innovation and R&D and technology capabilities, target market trends, industry trends, customer activities and end-market trends, market acceptance of Group technologies; increased competition; macroeconomic conditions; changes in laws, regulations or regulatory policies; and timing and success of strategic actions. These forward-looking statements speak only as of the date of this Presentation. As such, undue reliance should not be placed on forward-looking statements. Other than in accordance with legal and regulatory obligations, Alphawave IP undertakes no obligation to publicly update or revise any forward-looking statement, whether as a result of new information, future events or otherwise.

The Next Leader of Connectivity for AI

Tony Pialis, Co-Founder and CEO

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Leadership in Connectivity and Compute

Ultra-high-speed data connectivity for AI, compute and network architectures

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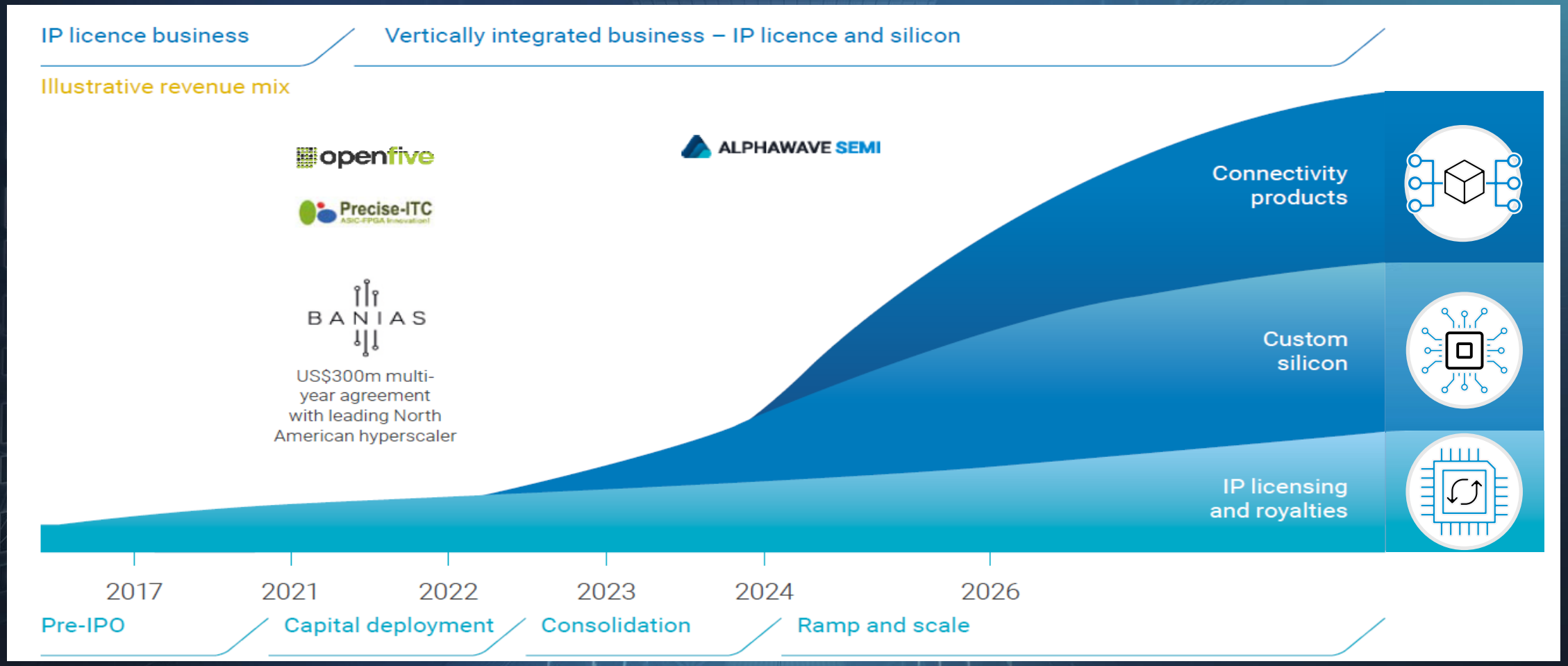
Delivering on our Vision: Leading Connectivity for AI and the Data Centre



Alphawave's technology leadership and track record since 2017 underpins our future growth

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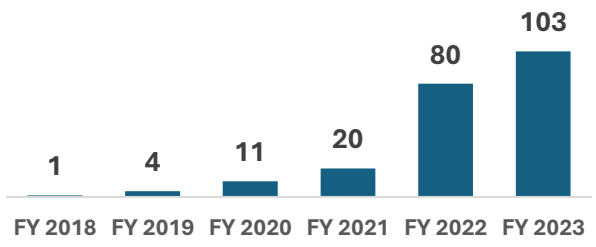
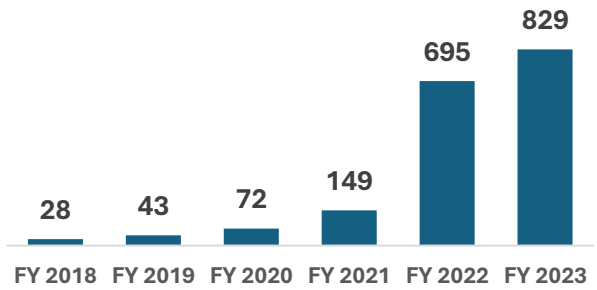
We Have Delivered Strong Growth Since Founding the Company in 2017

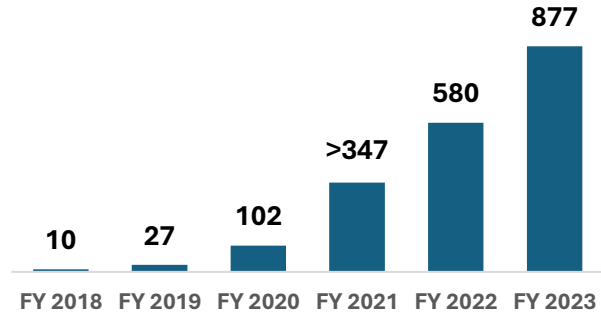
End Customers[1,2]



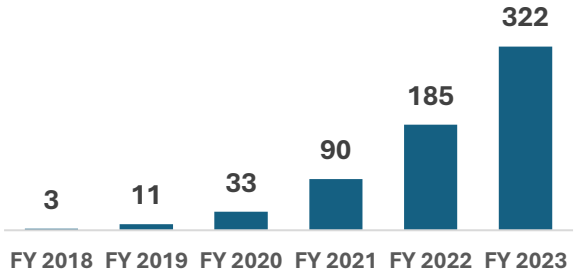
Employees[2]



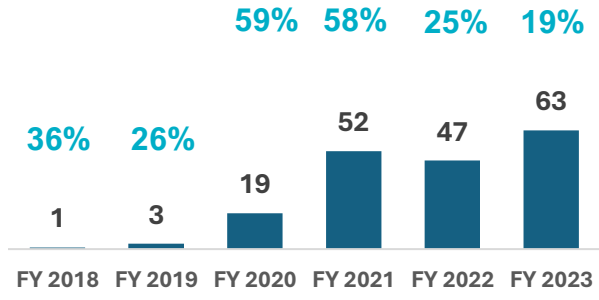
Cumulative Bookings[2] (US$m)



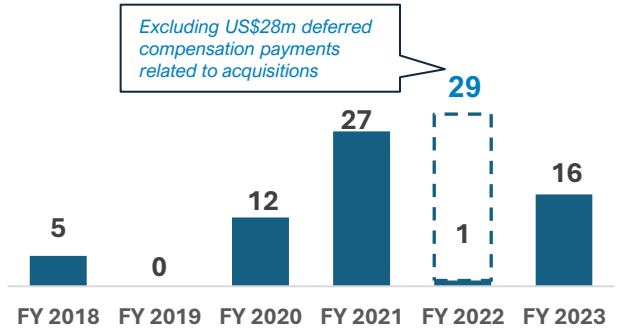
Revenue (US$m)[2]



Adjusted EBITDA[2] (US$m) & Margin



Cash generated from Operations[2,3,4] (US$m)



2024 is the year where we accelerate our growth as a vertically-integrated business

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1 Revenue generating customers.
2 FY 2018 as per IPO prospectus. FY 2023 includes backlog adjustment
3 FY 2022 has been restated
4 FY 2023 cash generated from operations restated to reflect capitalisation of interest incorrectly included in both interest payable and capitalised development expenditure in the FY 2023 cash flow statement

Leadership in Connectivity and Compute

Ultra-high-speed data connectivity for AI, compute and network architectures

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Relentless Growth in Data Consumption

AI at an Inflection Point

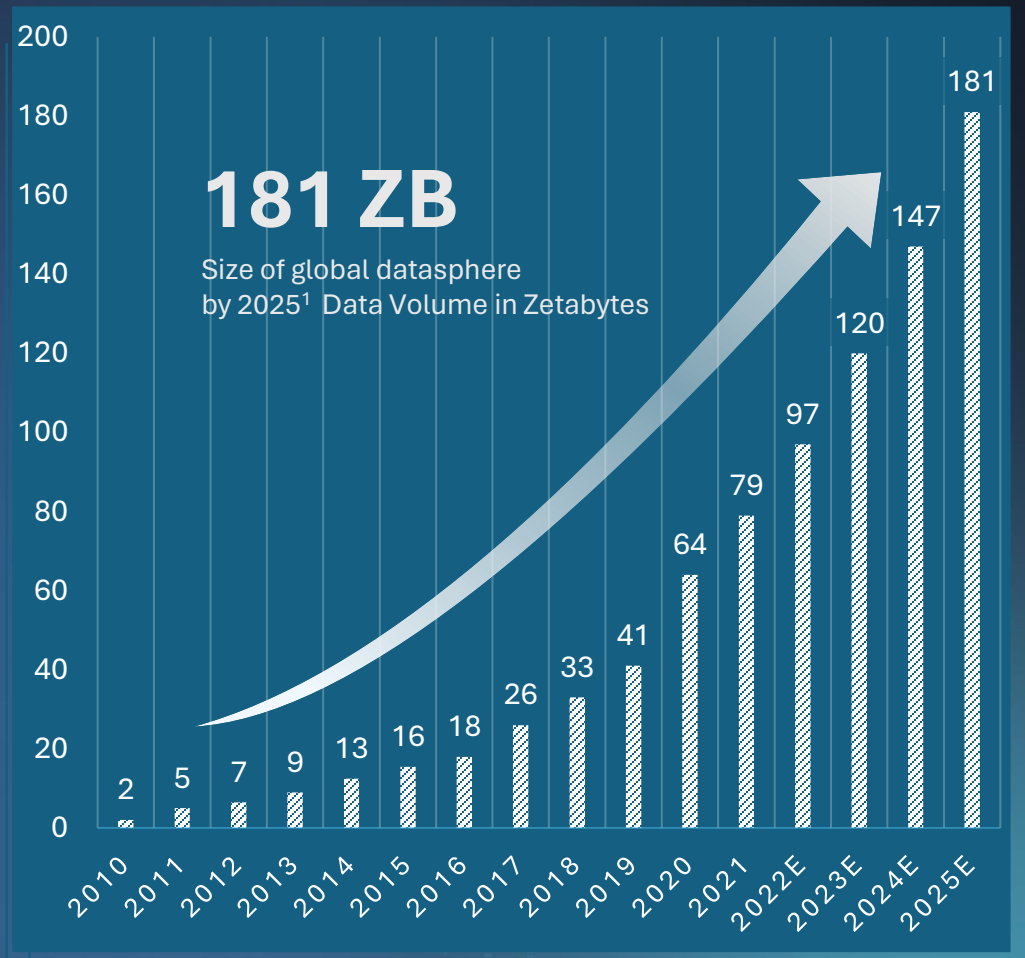
ChatGPT2.0
1.5 billion parameters
40GB data

ChatGPT3.0
175 billion parameters
45TB data
(one million feet of bookshelf space)

6-months prior, ChatGPT3.5 scored in the 37th percentile for the LSAT

ChatGPT4.0
trillion parameters
Text + Images

Completed in the 88th percentile of the LSAT



[1] The Data Centre Journey, From Central Utility To Centre Of The Universe (semiengineering.com). Source Statista
See slide 93 for all other references

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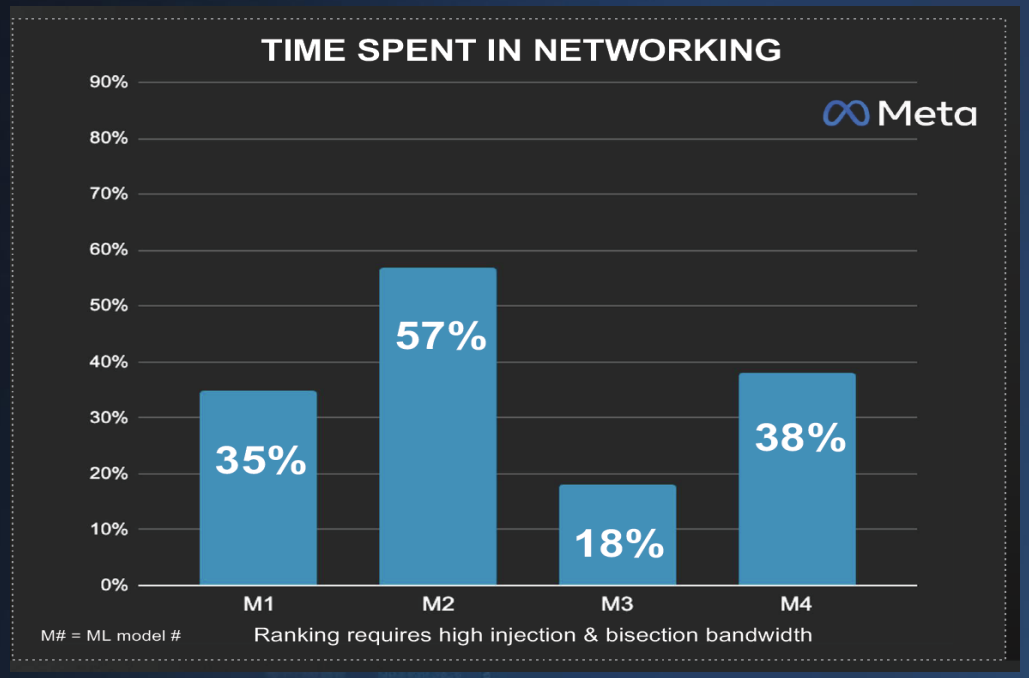
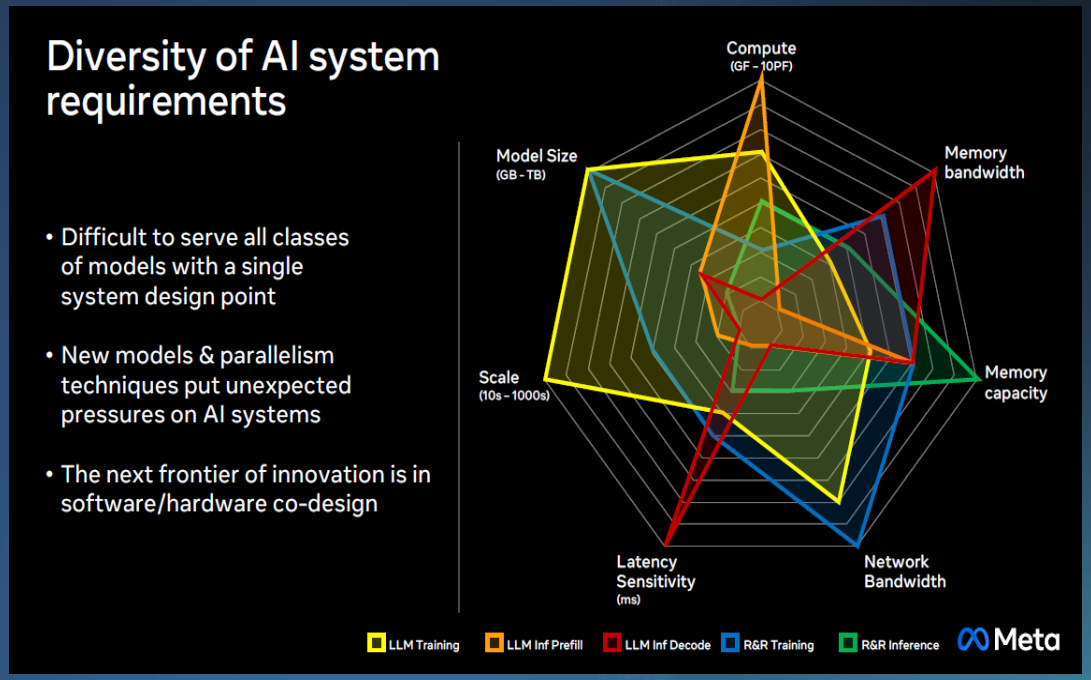
…Drives Challenges for AI and The Data Centre

Connectivity



Custom Compute



Source AI Summit : “Leading with Open” Meta

AI requires dedicated hardware with maximum communication bandwidth

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Data Centre Infrastructure is Pushed to the Limits

General Purpose GPU FOR AI: Hitting Limits

Silicon limit - Compute has hit a wall

Single training of Chat Gpt3 released 552 tons of CO2

$100s of millions per training

Investment Needed to Deploy ChatGPT Across Bing

$4 billion

8 GPUs per server ✖ **20,000 servers** ✖ **$10k-$30k cost of each GPU**

* Estimate from New Street Research

US Data Centres expected to consume 30GW incremental power by 2030

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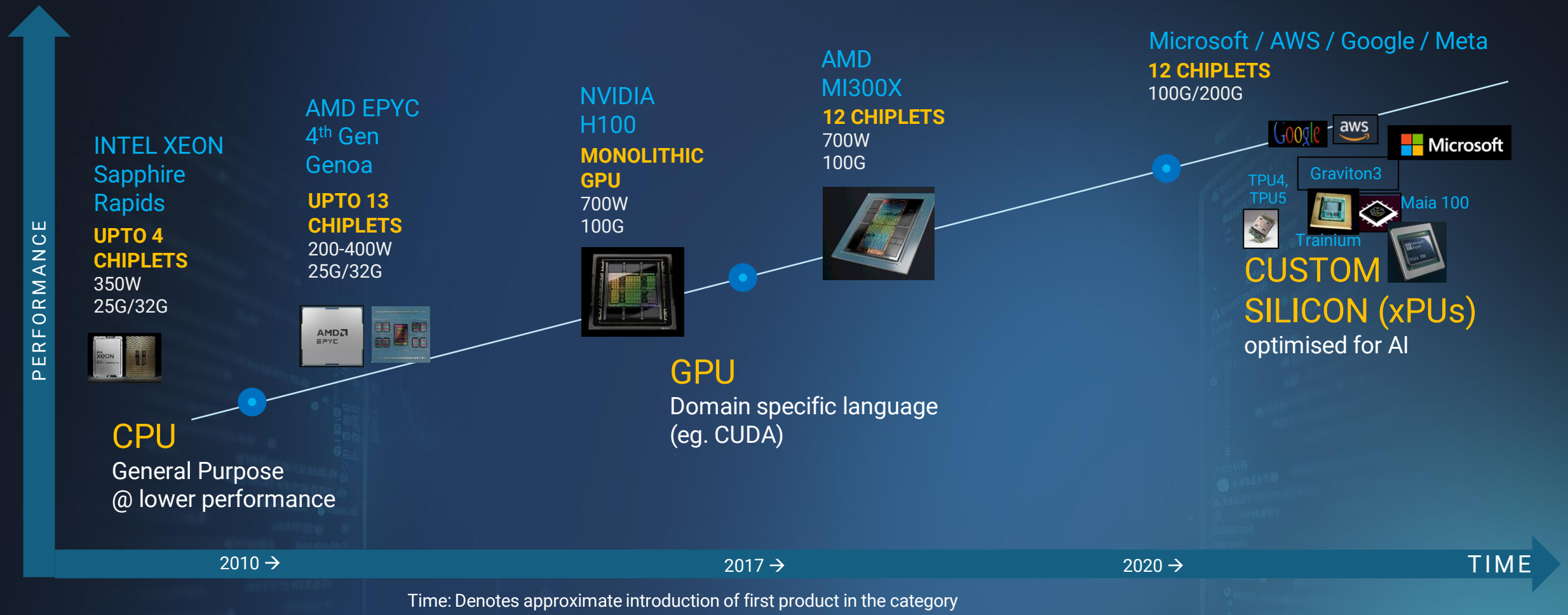
The Result: Evolution of Silicon for AI



Time: Denotes approximate introduction of first product in the category

Until now – No one solutions provider possessed all of the technology to enable silicon for AI

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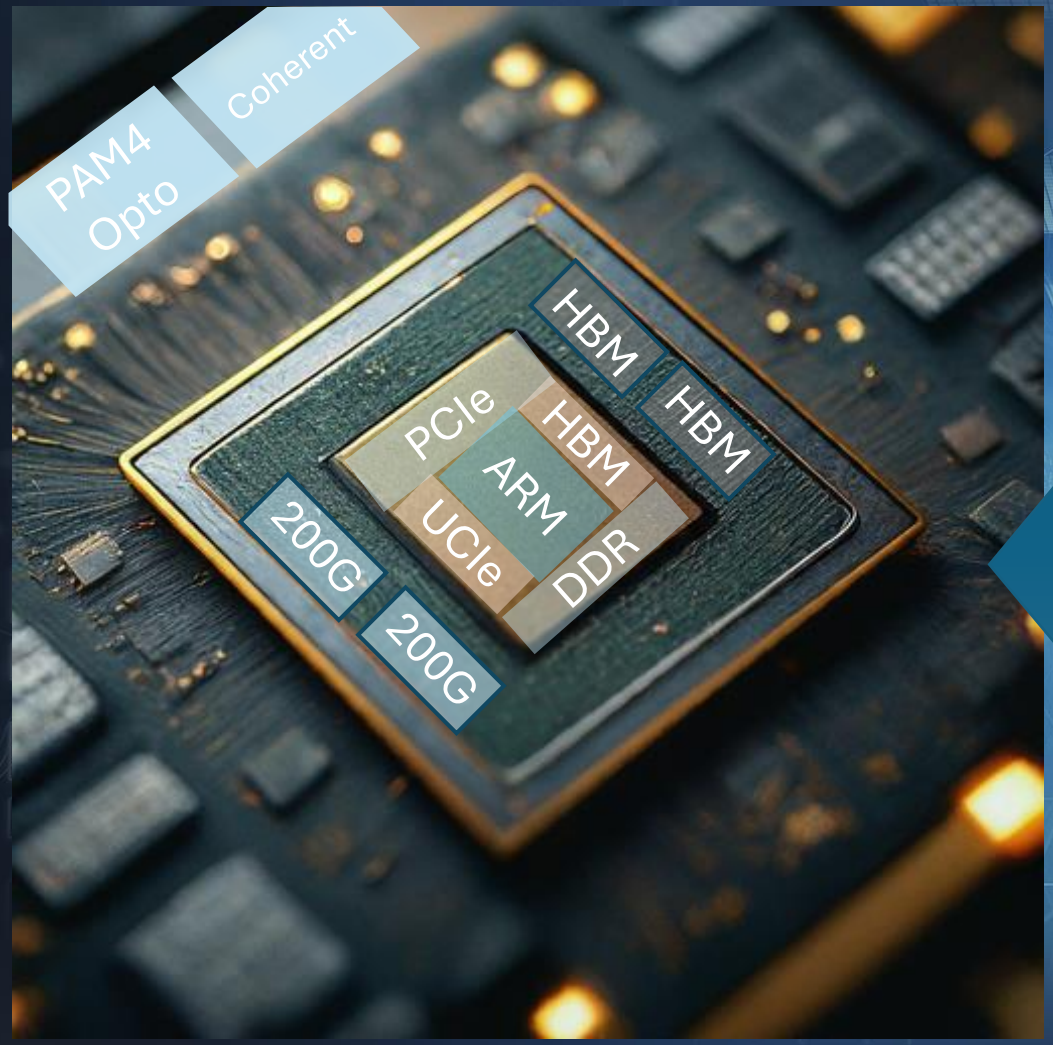
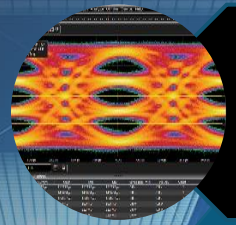
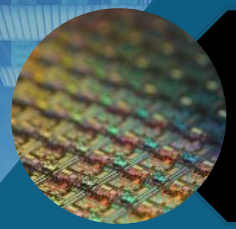
Alphawave Has The Complete Silicon Solutions Stack





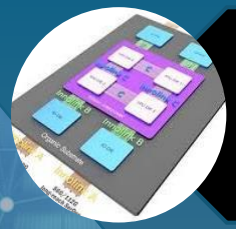
Silicon IP

- PCIe / CXL
- 224G / 112G Ethernet
- UCIe / HBM



Custom Silicon

- 5nm, 4nm, 3nm and 2nm Nodes
- 2.5D and 3D advanced packaging
- ARM Total Design Partner



Chiplets

- IO Extender Chiplets
- ARM Neoverse Compute Chiplets
- Memory Chiplets

Connectivity Products

- PAM4, Coherent DSPs for 800G/1.6T Ethernet
- 112G, 224Gbps in silicon
- Going to 400G

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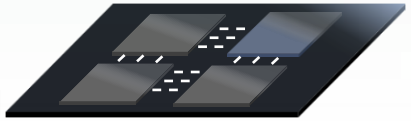
Chiplets - Next Evolution of Silicon IP

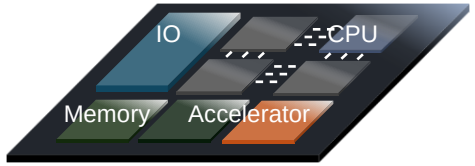
New Chiplet Design Paradigm

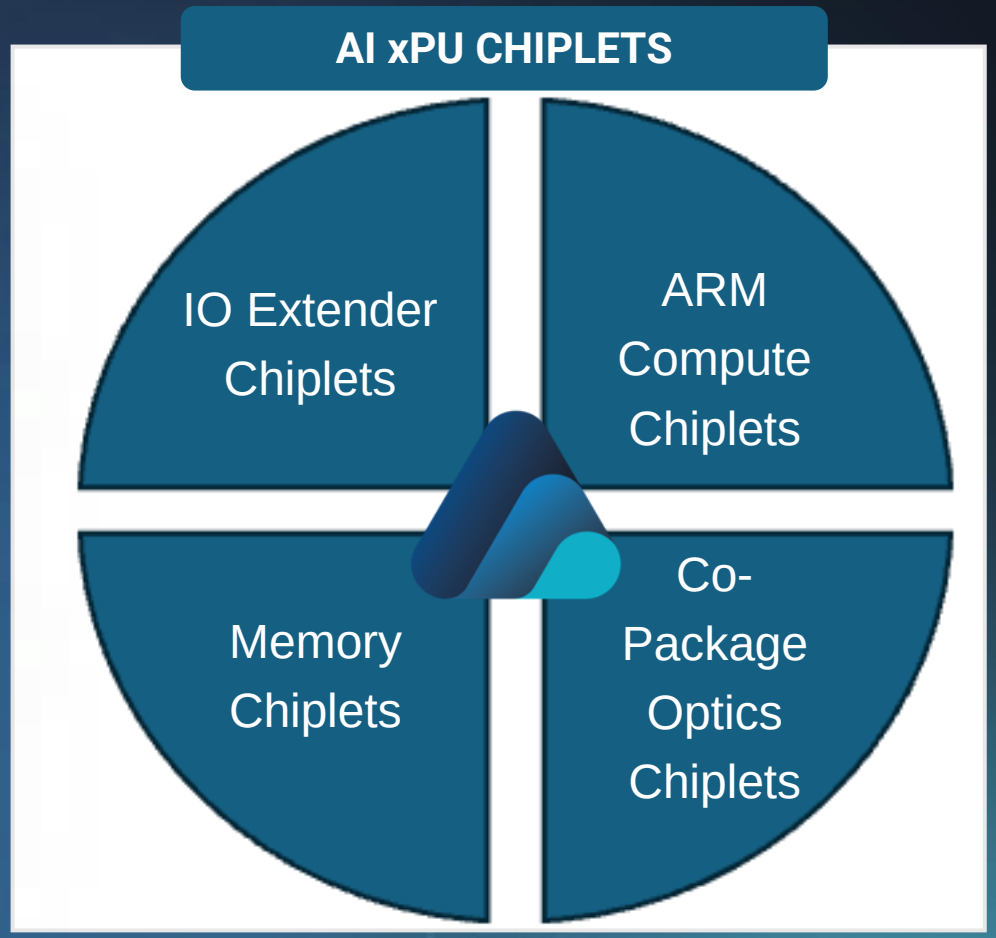
Monolithic is costly for AI and Data Centre in 3/2nm nodes

Chiplets with 2.5D/3DIC allow for greater compute and memory scaling



Customisable IO and Compute Chiplets Accelerate Time to Market





Partnering with ARM to deliver a portfolio of Neoverse series compute and IO Chiplets

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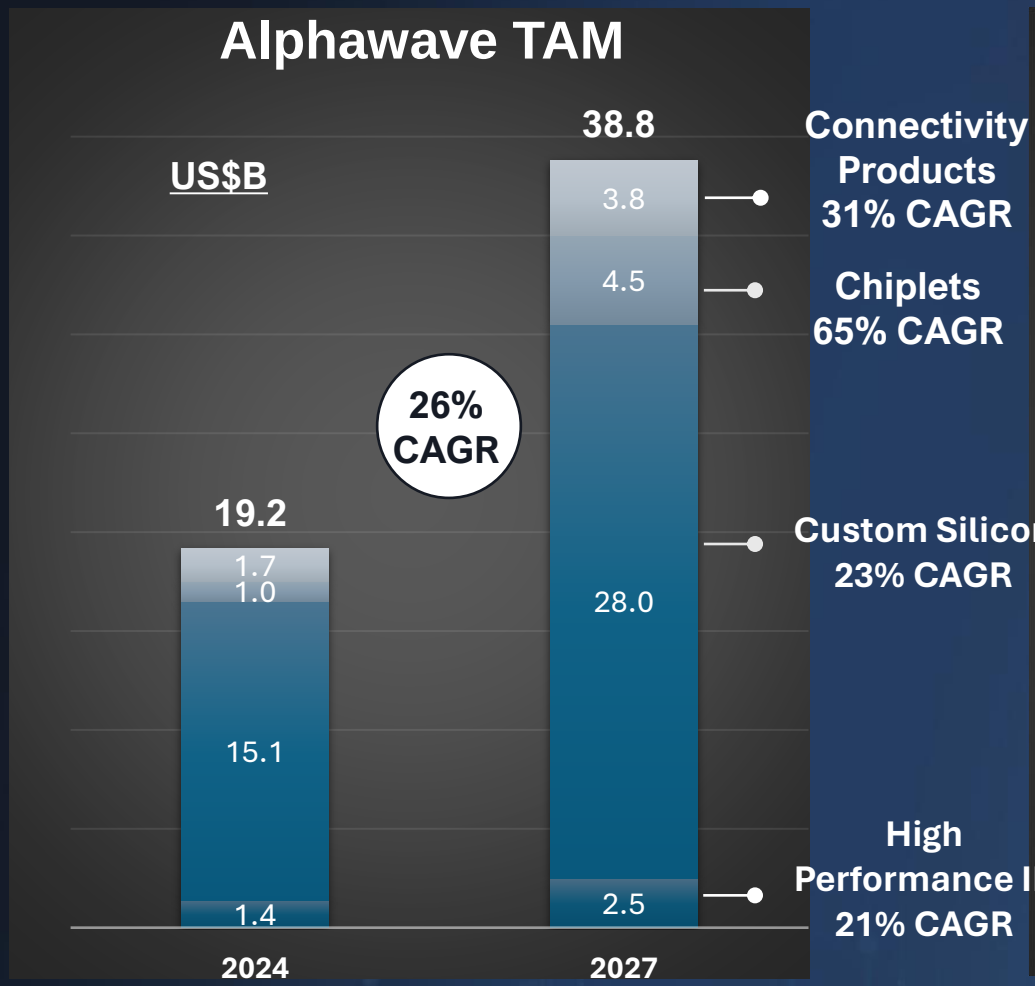
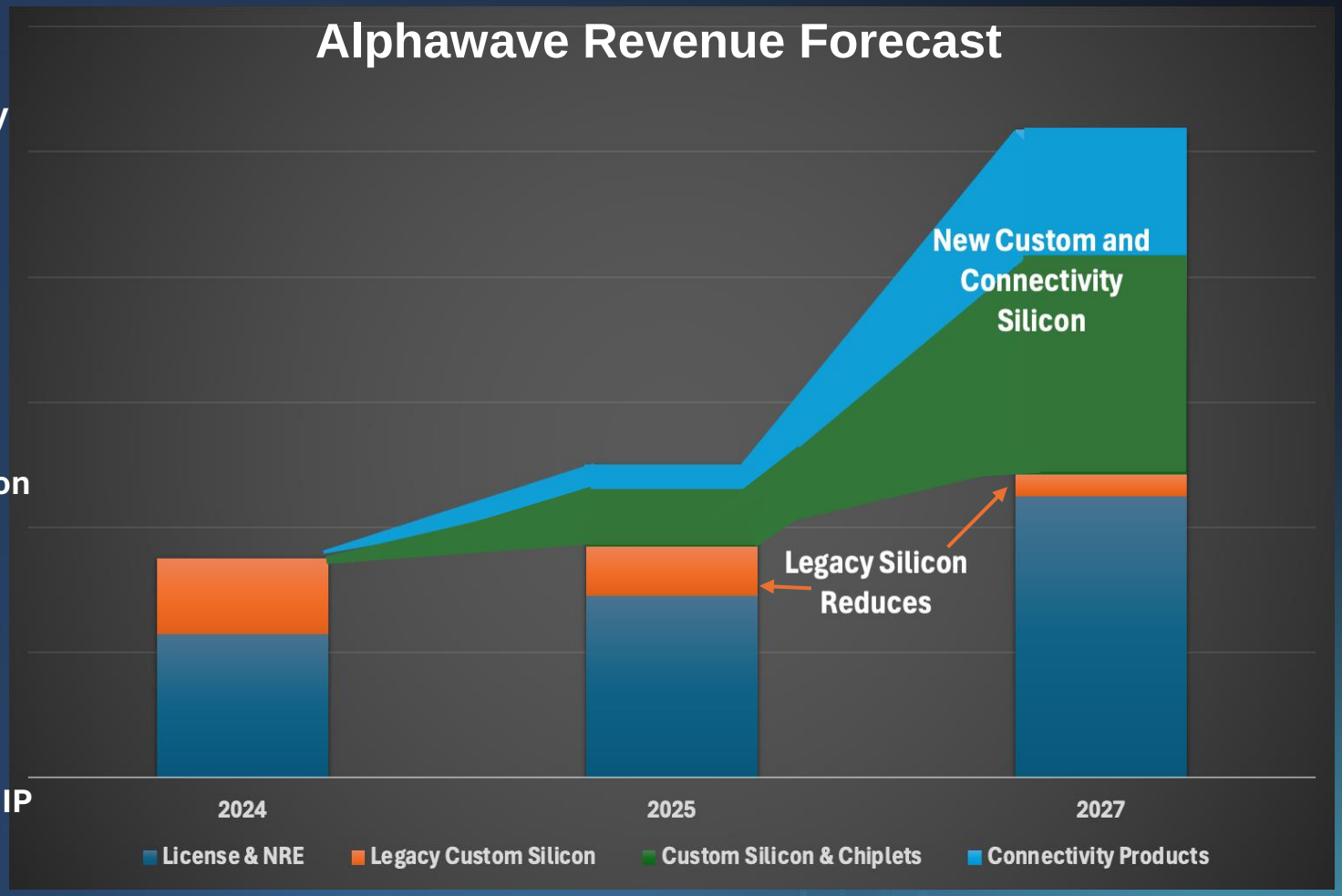
Alphawave Accelerates the AI “Industrial Revolution”





More than $1B of silicon revenue potential from existing wins

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Strengthening our Leadership and Governance

Execution in 2023

- **Management Focus:** Expanded and enhanced management team
  - Rahul Mathur: CFO
  - Charlie Roach: CRO + MARCOM
- **Efficiency Focus:** Began implementation of ERP system to drive more efficient integration
- **Governance Focus:** Began Board re-alignment to focus on core markets and capabilities

Execution in 2024 & Beyond

- **Capital Structure Focus:** Simplify our debt to maximise balance sheet strength while driving opportunities and flexibility
- **WiseWave Equity Sale:** Further strengthen balance sheet with WiseWave equity exit
- **Governance Focus:** Expand diverse Board capabilities in our key markets of AI and the Data Centre

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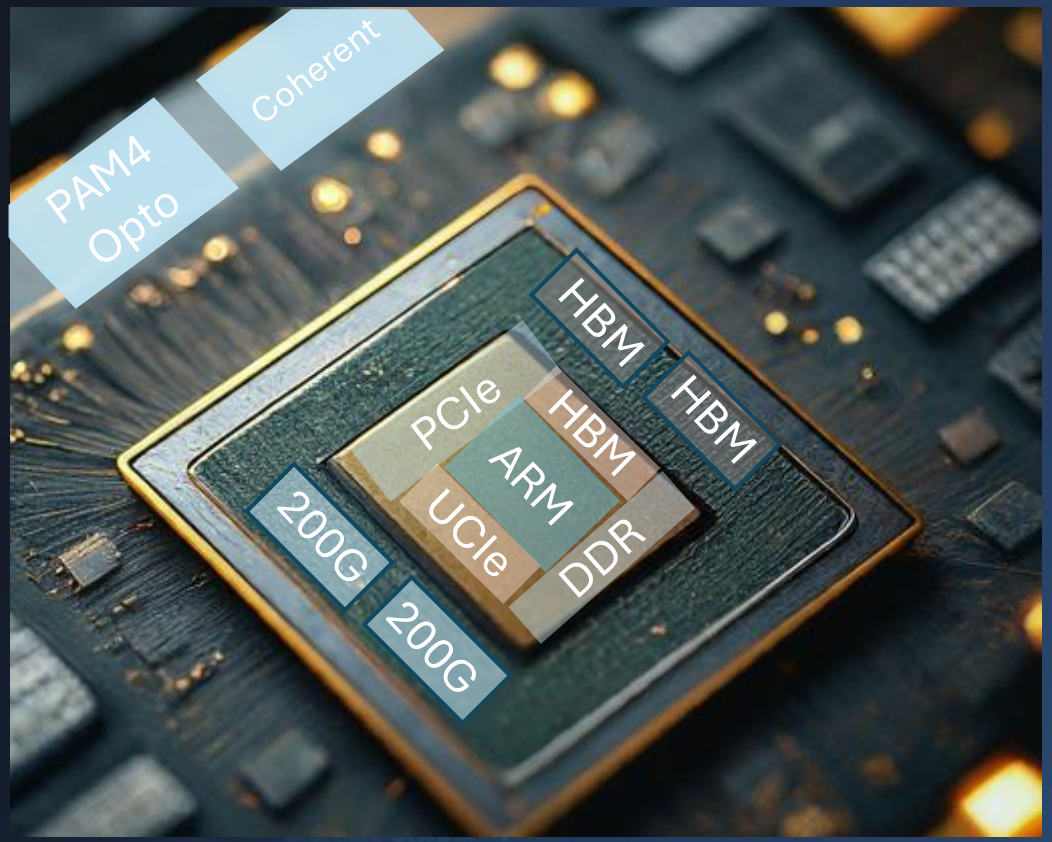
Leveraging Our Core Strengths to Increase Value



- Delivering leading technologies to AI
  - Built via chiplets and powered by custom silicon
  - Connecting high bandwidth optical and electrical fabrics for AI
- Disciplined investment in R&D to fuel further growth in high-margin products
- Expanding shareholder value through business delivery and balance sheet strengthening

We will deliver revenue at significantly enhanced scale, and at higher profit – Driving outsized shareholder value in 2024 and beyond

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AI and Data Centre Megatrends

Tony Chan Carusone, CTO

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Leadership in Connectivity and Compute

- Silicon IP
- Custom Silicon
- Chiplets
- Connectivity Products

Ultra-high-speed data connectivity for AI, compute and network architectures

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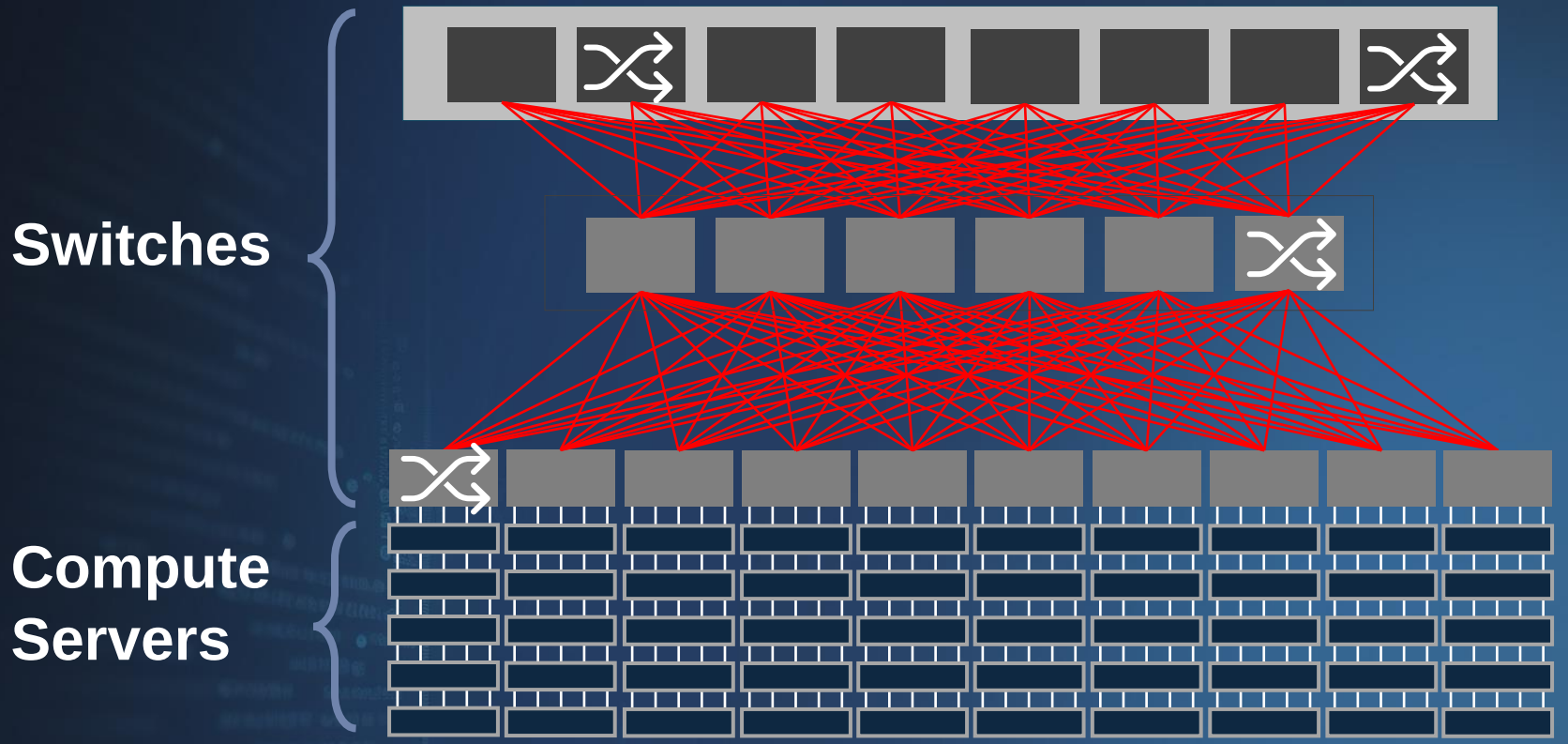
Evolving Data Centre Connectivity Landscape



- Optical and electrical links
- Flexible and redundant networking

This evolution is accelerating and diversifying with AI deployment in the data centre

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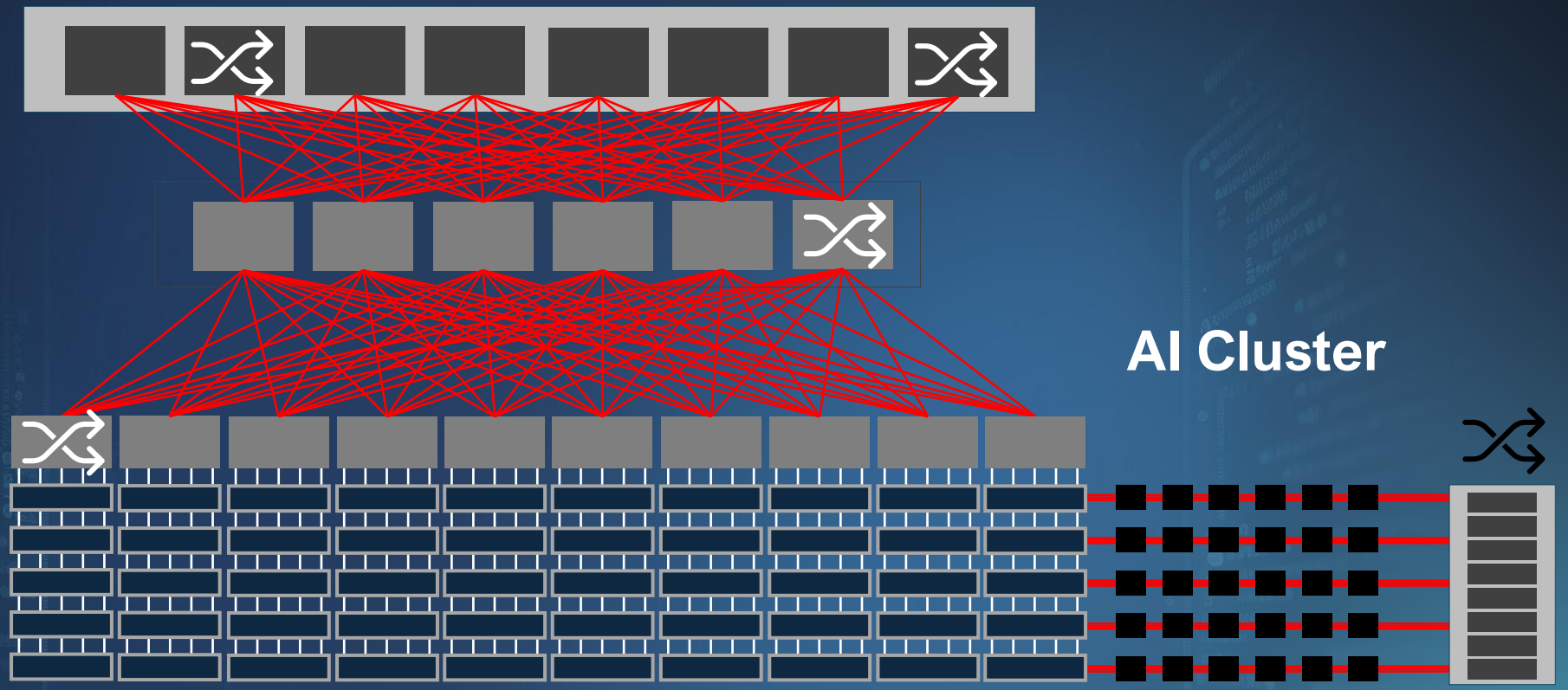
Proliferating Connectivity – AI in the Data Centre

Front-End Data Centre Network



AI Cluster

Back-End ML Network

- Low-latency & high-speed

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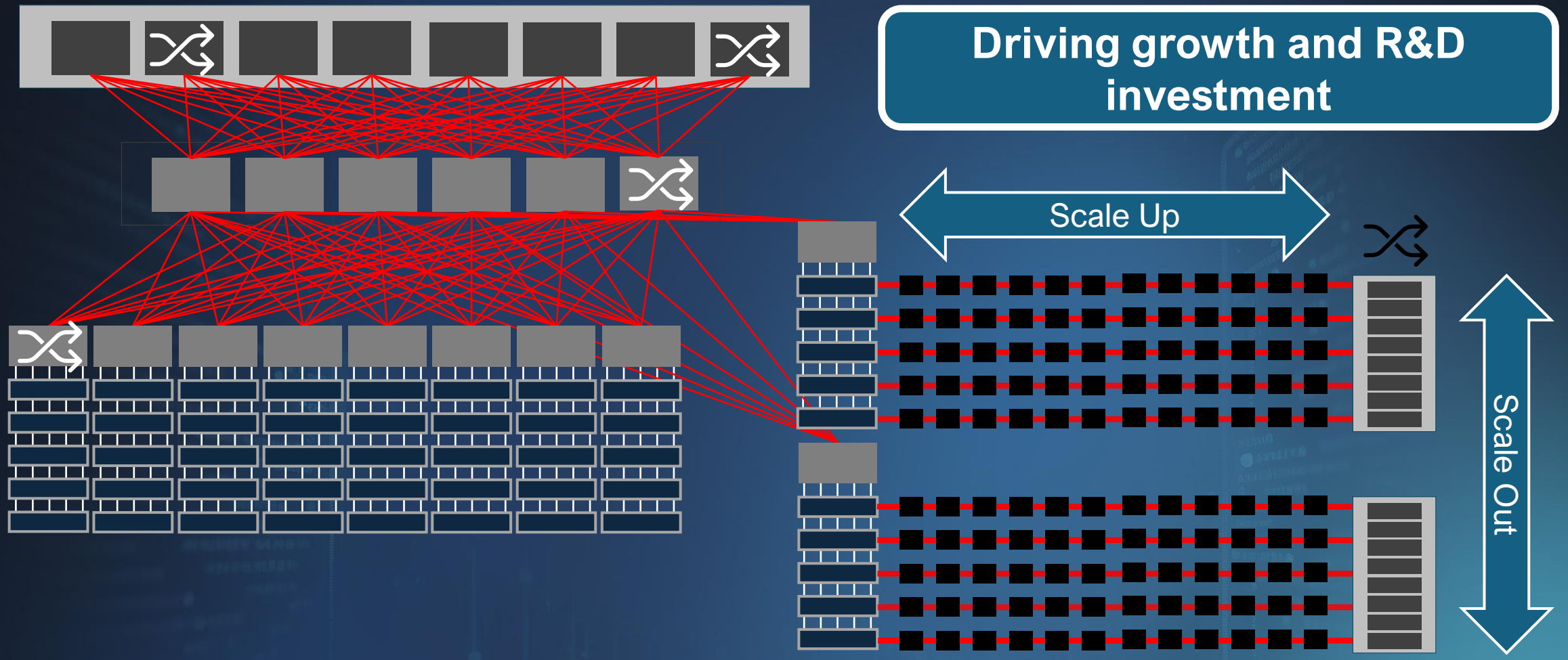
Driving Large-Caliber Scaling Up and Scaling Out



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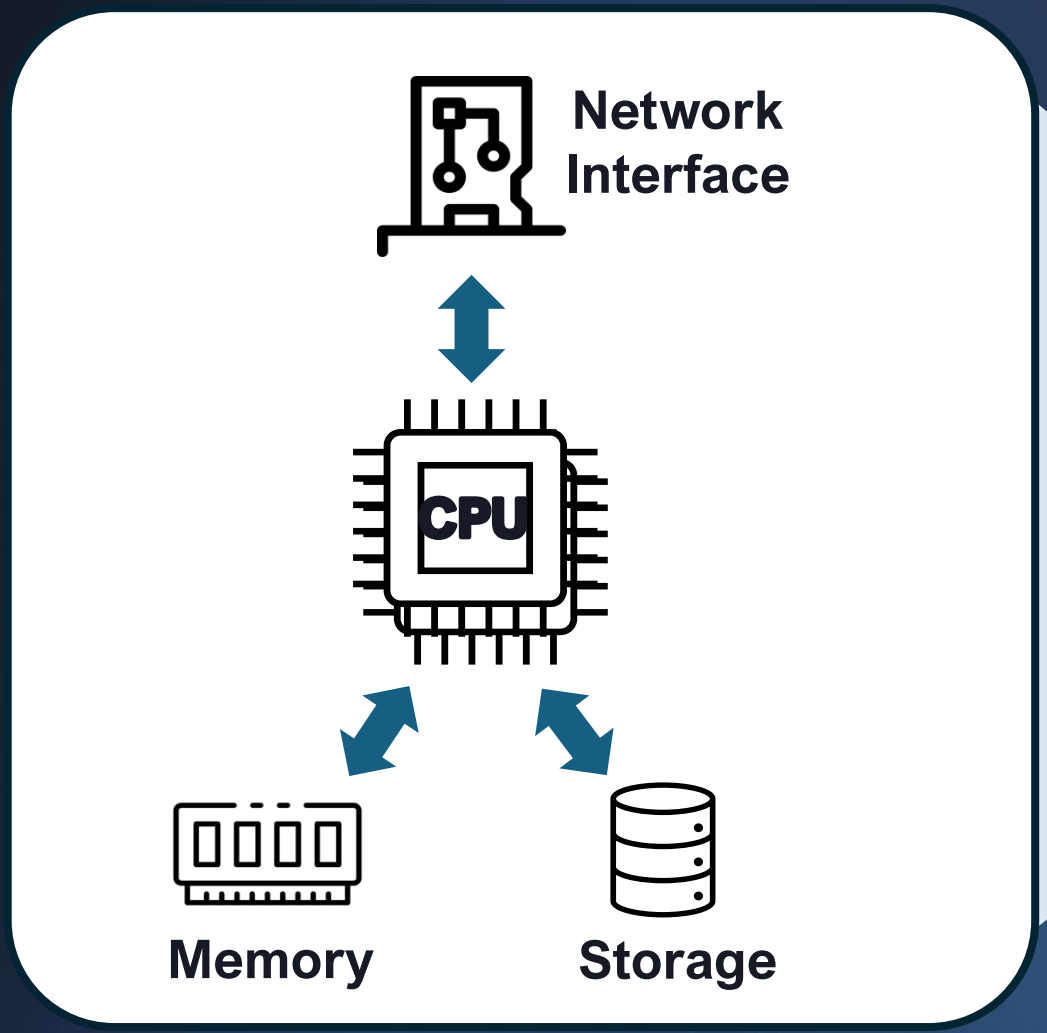
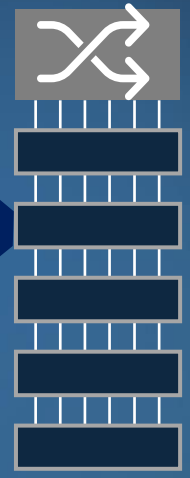
Building the Modern Data Centre – Compute Nodes



- Traditional compute server



Compute Servers

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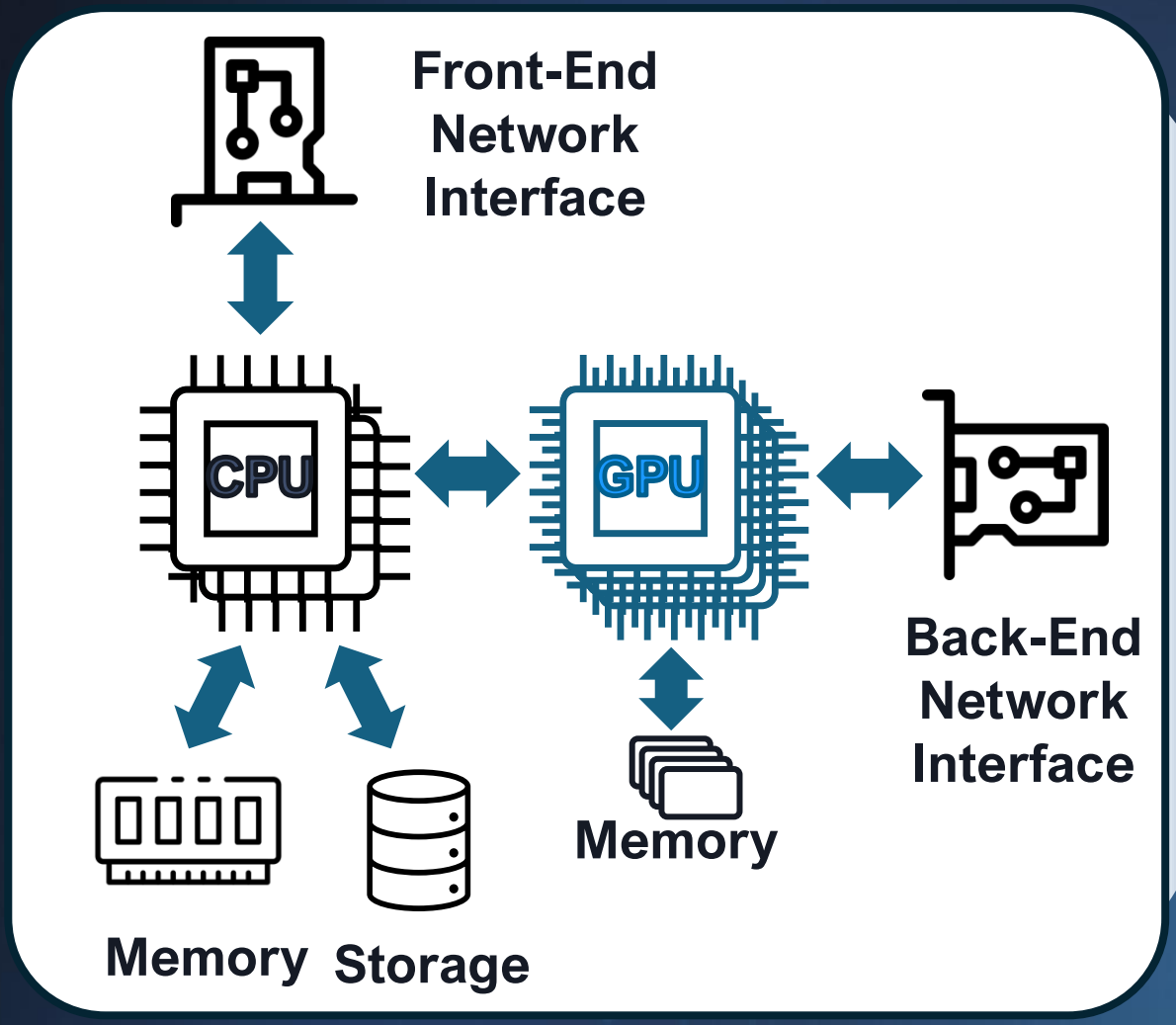
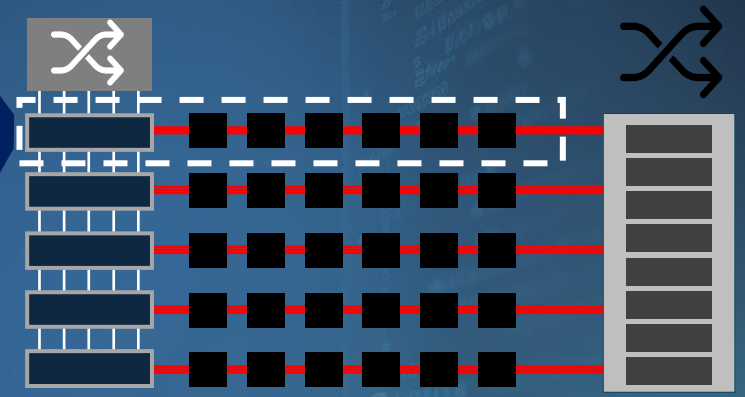
Building the Modern Data Centre – AI Compute Nodes



- Evolved for AI



Back-End ML Network

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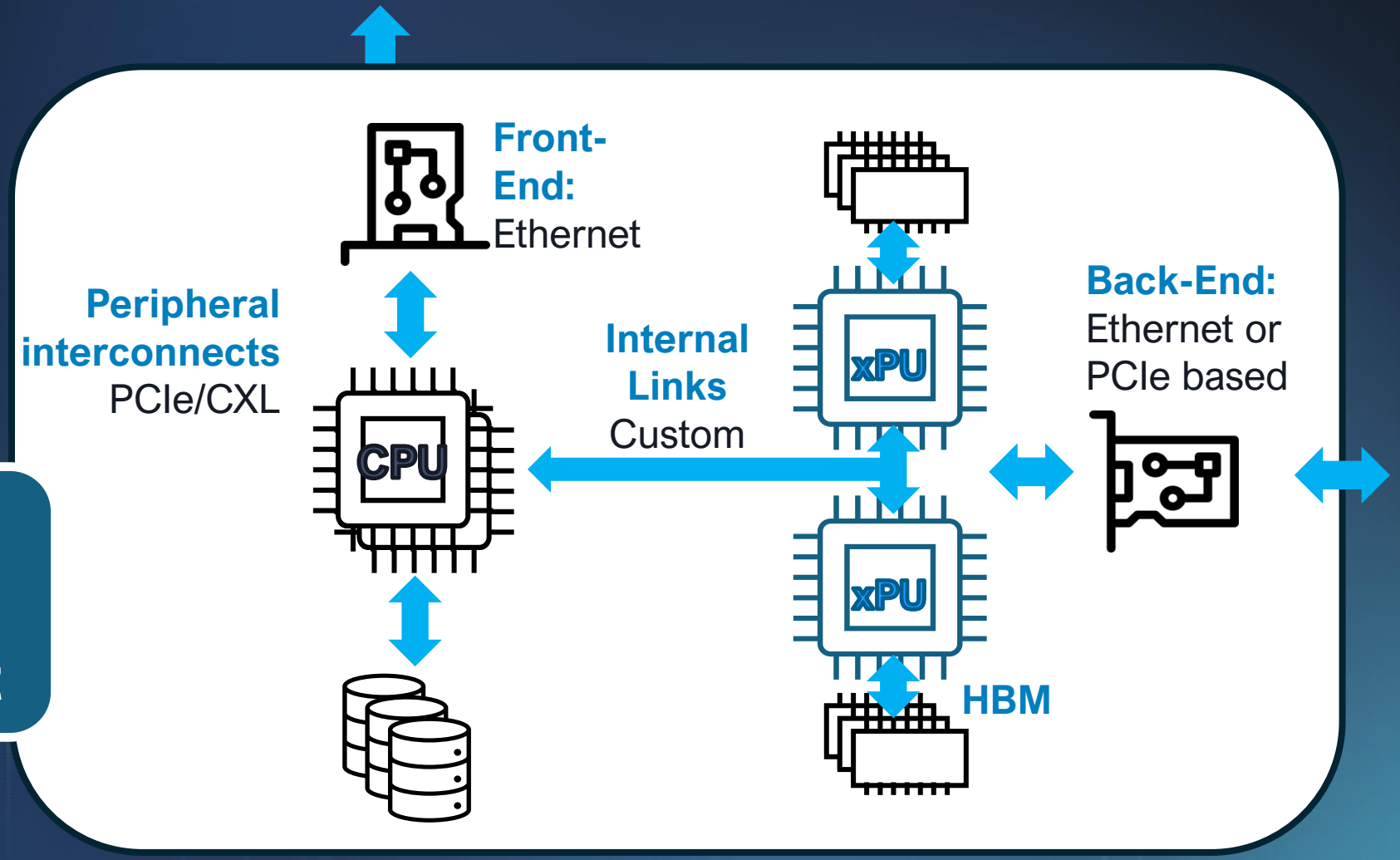
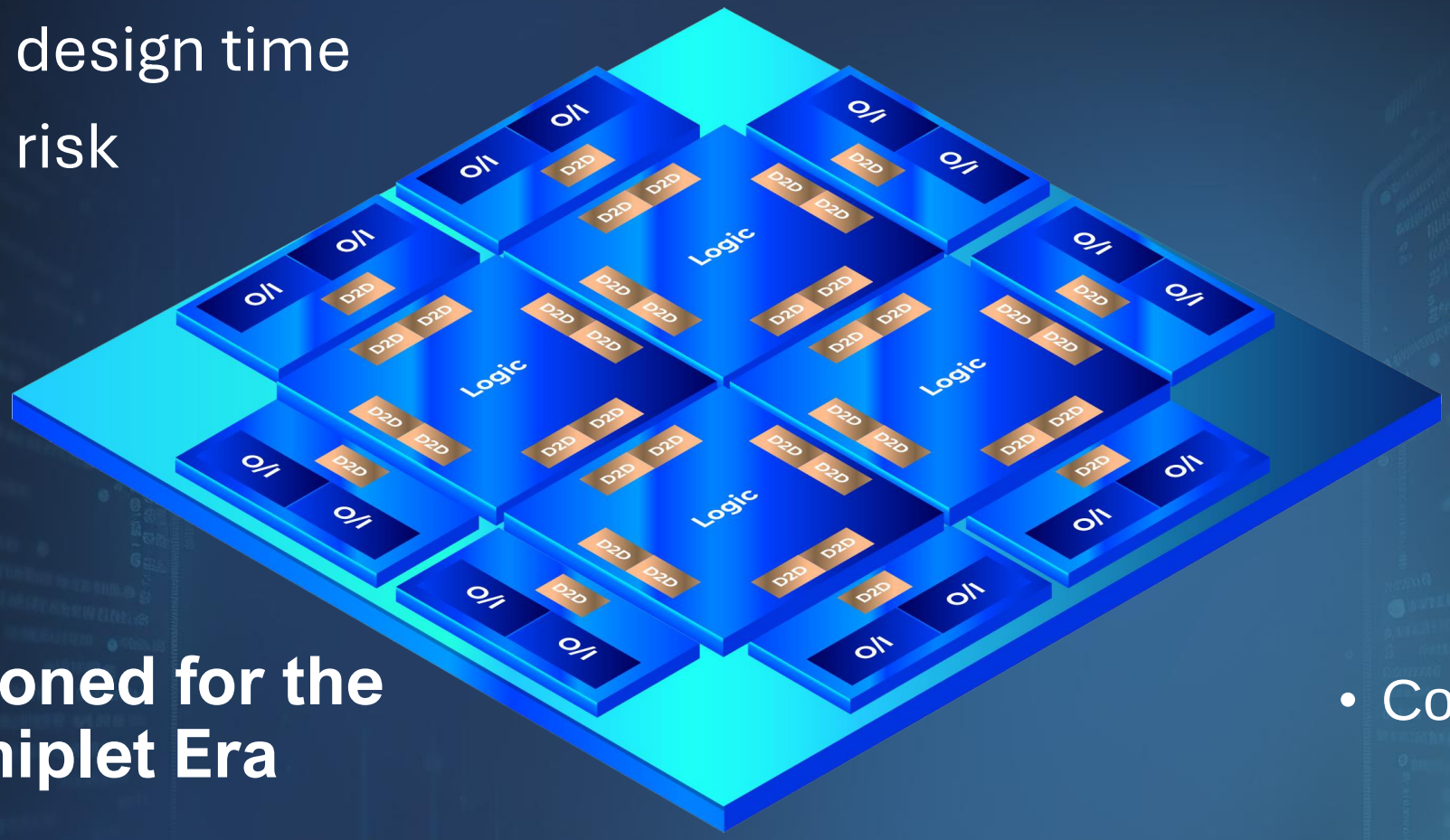
Alphawave Delivers the Full AI Connectivity Suite

Alphawave Solutions Throughout



Accelerating the Cadence of Hardware Upgrades

- Reduced design time
- Reduced risk



Positioned for the Chiplet Era

- Composability

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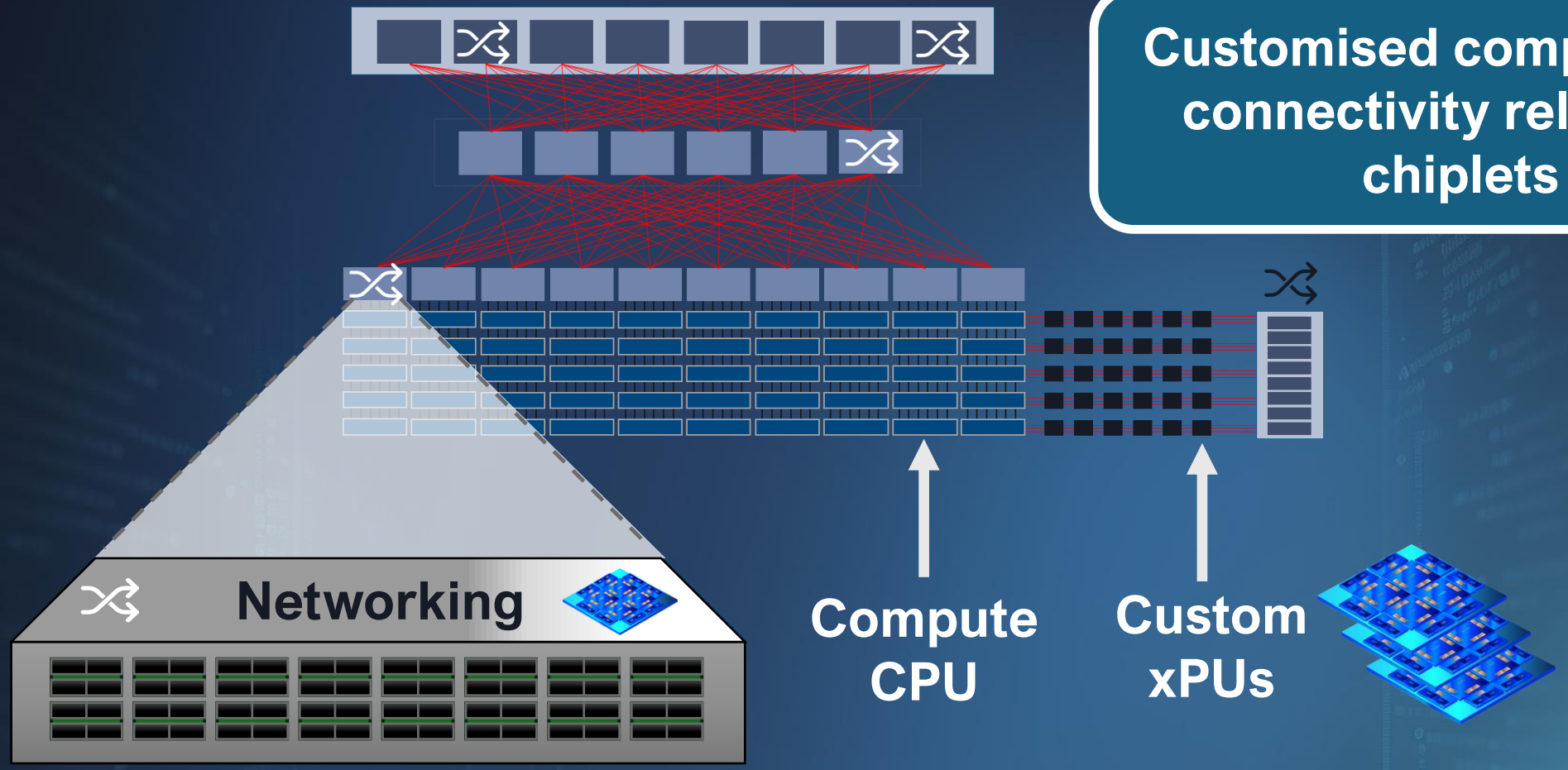
Delivering Custom Silicon in the Data Centre



Customised compute and connectivity reliant on chiplets

This presents new challenges for the networking infrastructure

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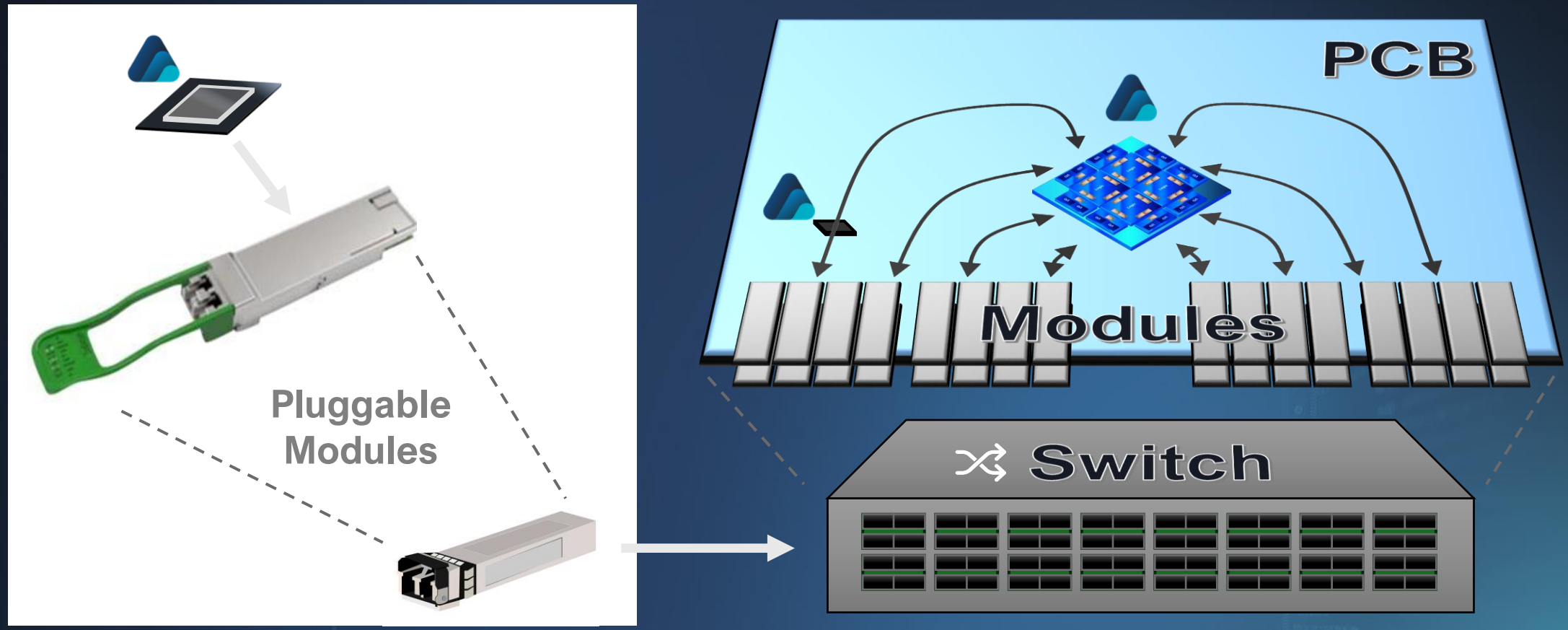
Alphawave has Solutions for These Networking Challenges



Industry-leading technology in volume deployment

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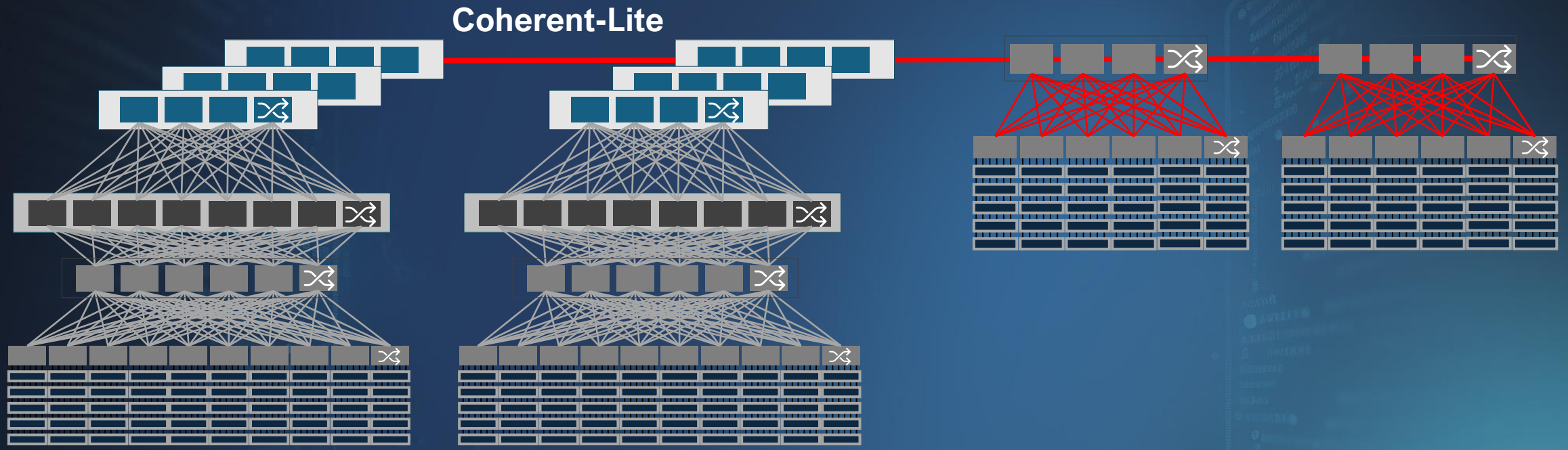
Evolution of Distributed Compute Drives New Requirements

AI at the edge requires geographically-distributed compute with broadband connectivity



Future solutions are needed to address these new requirements

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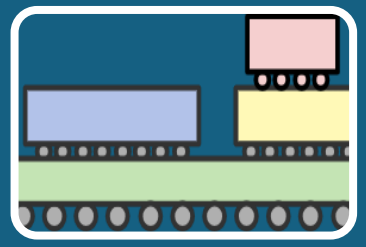
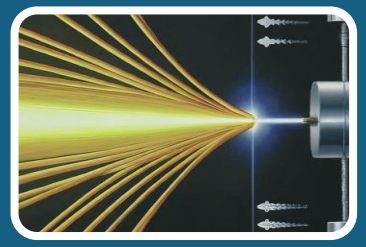
Alphawave is Investing in These Future Solutions



3D Silicon

Beyond 224G Connectivity



Coherent in the Data Centre

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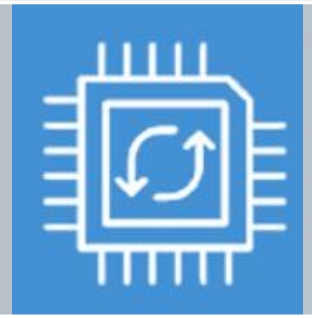
Alphawave is Expanding Technology Leadership



Alphawave's AI connectivity suite is enabling custom silicon:

- PCIe/CXL
- Ethernet
- UCIe / HBM

Alphawave chiplets are scaling AI in composable compute and networking chips

Optics technologies are evolving to meet new demands

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Alphawave R&D

Jonathan Rogers, Co-Founder and Senior Vice President Engineering

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Leadership in Connectivity and Compute

Ultra-high-speed data connectivity for AI, compute and network architectures

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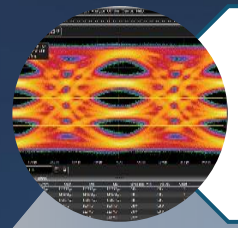
R&D Engine Powering our AI and Data Centre Connectivity Businesses

R&D Locations

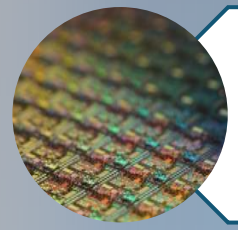
Leading experts in analog mixed-signal and DSP design

Team members with decades of experience building connectivity solutions



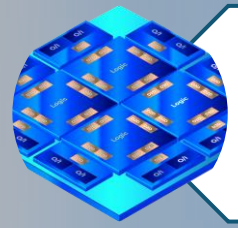
High-Speed Connectivity IP

- Data Rates up to 224Gbps
- Most advanced silicon processes
- Robust production track record



Driving Custom Silicon Business

- Full suite of proven differentiated IP subsystems for AI connectivity and compute challenges



Chiplet Innovation

- 2.5D/3D advanced package expertise
- UCIe leaders at 32Gbps

Connectivity Products

- Directly driving optics from advanced CMOS
- WidEye™ DSP

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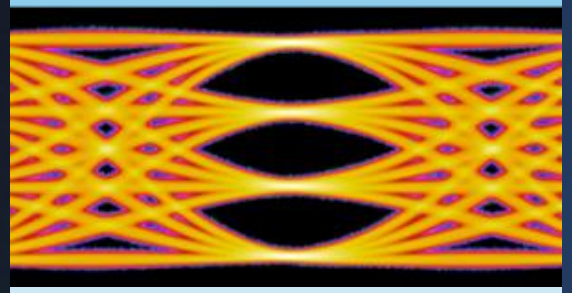
Driving Evolution of IP at Alphawave

Transceiver IP



- Ethernet Transceiver
- PCIe Transceiver
- UCIe Transceiver
- HBM Transceiver

Pre-Validated Subsystems

Subsystem

Transceiver IP | Controller IP

- Ethernet Subsystem
- PCIe Subsystem
- CXL Subsystem
- UCIe Subsystem
- HBM Subsystem

Chiplets

Chiplet

Subsystem A

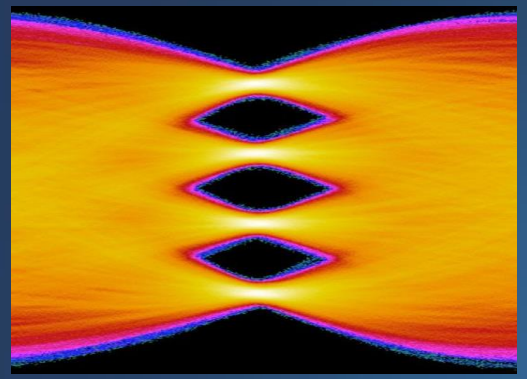
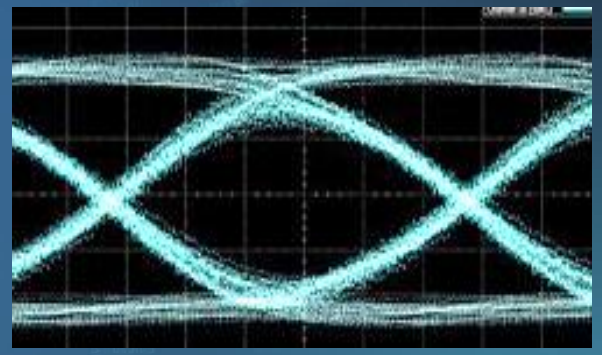
Subsystem B

- PCIe + UCIe Suite
- Ethernet + UCIe Suite

Alphawave has the transceivers, controllers and pre-validated subsystems for the AI data centre

ALPHAWAVE SEMI

Building Differentiated Connectivity IP

Our Connectivity IP Enables	224Gbs AthenaCORE SerDes	24Gbs AresCORE UCIe
Faster Speeds		Low-Latency Streaming Controller
Lower Power	WidEye™ DSP	
Lower Cost		

Delivering higher speeds, better performance for less power and area

ALPHAWAVE SEMI

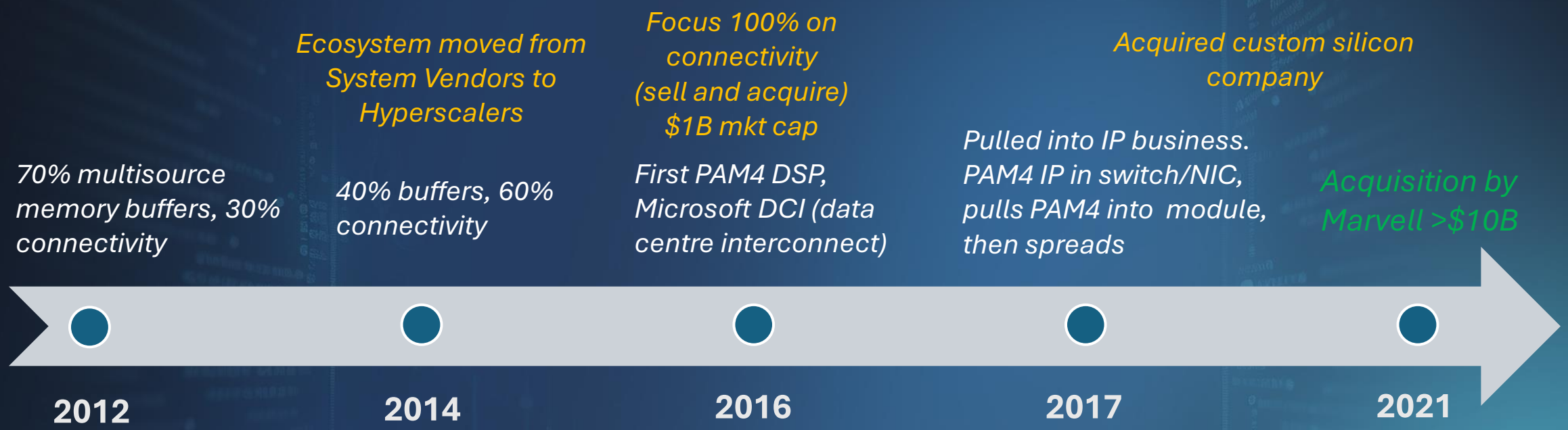
Path to Billions

Charlie Roach, Chief Revenue Officer

ALPHAWAVE SEMI

Connectivity Technology Creates Value

Inphi Worldwide Sales 2012-2021



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Leadership in Connectivity and Compute

US Hyperscalers >50% of TAM

Ultra-high-speed data connectivity for AI, compute and network architectures

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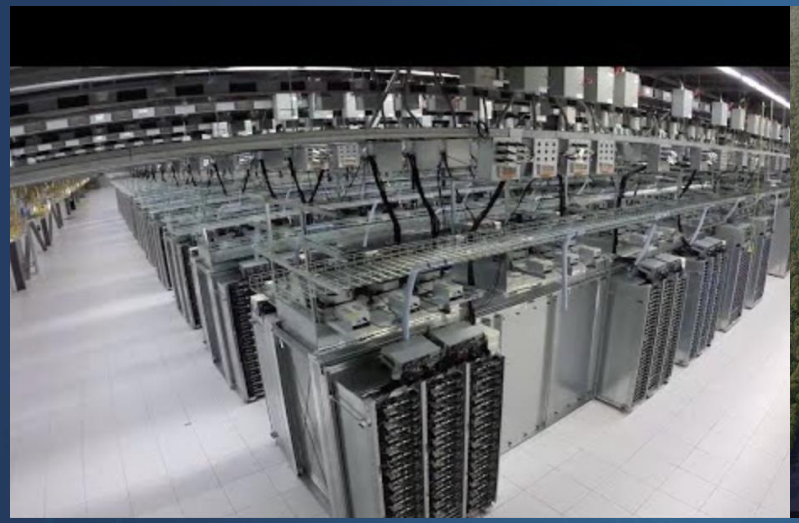
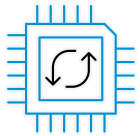
How Alphawave Wins: Technology Leadership

- For Hyperscalers, proven cutting edge connectivity technology wins
  - Connectivity of silicon from millimeters apart, to meters, and kilometers
  - Prefer technology from same company to de-risk mass deployment
  - Alphawave is the only complete connectivity supplier for IP, Custom Silicon, Chiplets and Connectivity products
  - Competition sells IP or silicon



ALPHAWAVE SEMI

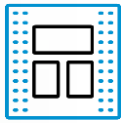
Four *Connected* Entry Points for Alphawave



Silicon IP

High Performance Connectivity IP

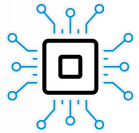
- PCIe/CXL
- Ethernet
- HBM



Chiplets

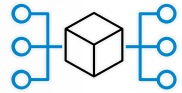
UCIe™ Enabled

- IO Chiplet
- Memory Chiplet
- Compute Chiplet



Custom Silicon

- Spec to Silicon Capabilities
- Advanced 2.5D/3D Packaging
- Application Optimised IP Subsystems



Connectivity Products

IPAM4 and Coherent DSPs

Enables selling across the entire product portfolio – Directly or Ecosystem

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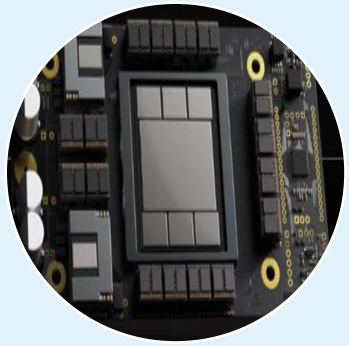
Creating the Solutions Hyperscalers Specifically Request

Alphawave Is Working with the Entire Hyperscaler Ecosystem

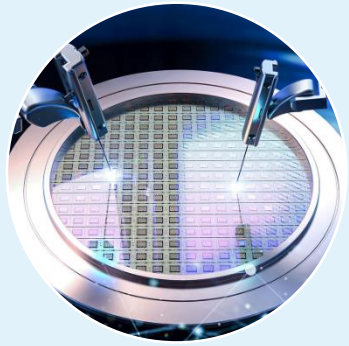
Module/Cable Vendors

- Copper and optical module vendors



Data Centre Compute

- AI, speciality processors and connectivity solutions



Silicon Fabs

- TSMC, Samsung and Intel

Compute Architecture

- Compute architecture partners such as ARM

Hyperscalers Require Industry-Leading Standard Technology that is Customisable

Google Cloud Platform

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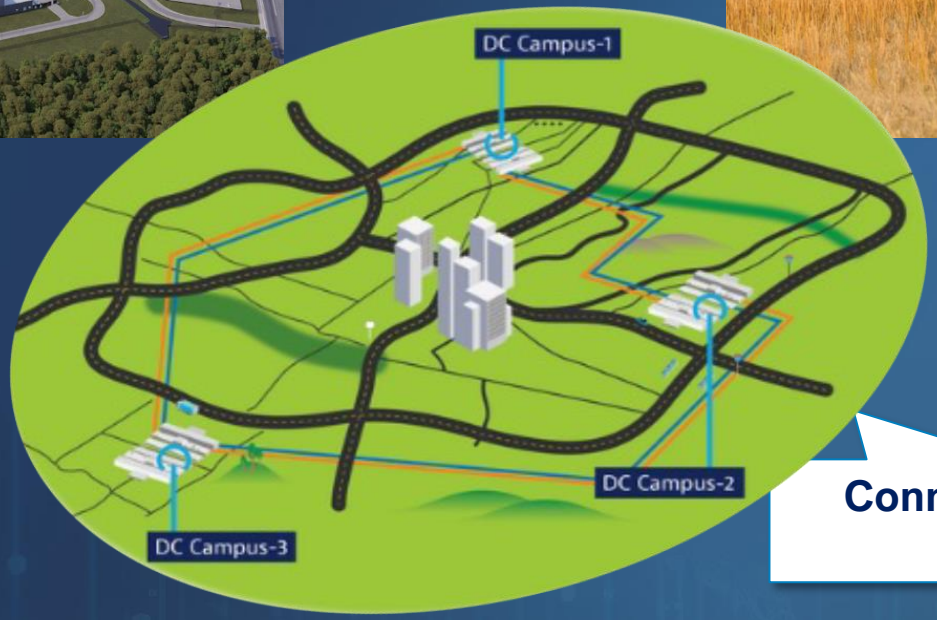
Diversification of Data Centres

Think Phone vs Tablet vs Laptop

Campus connecting several buildings

Large single building in remote location



Connected campuses around city

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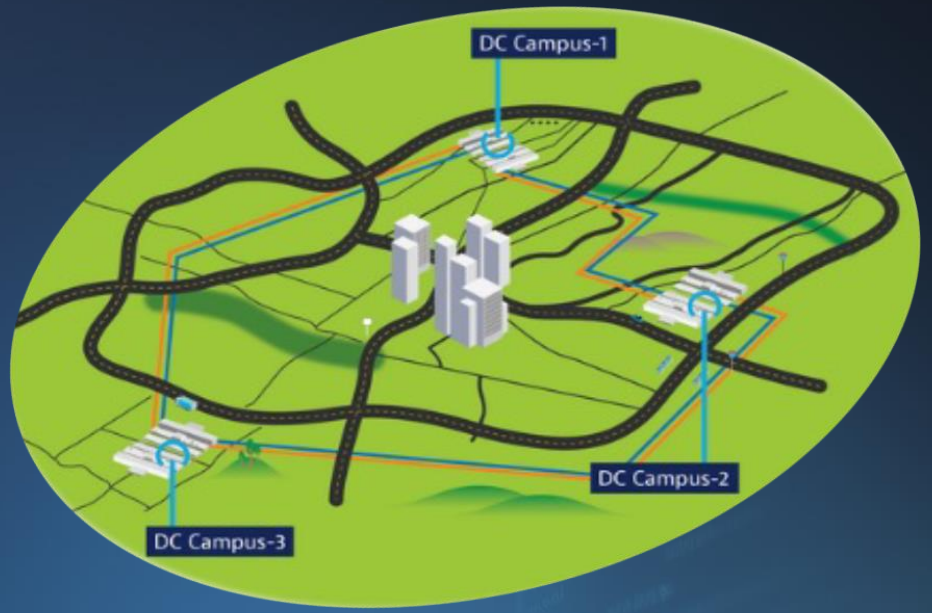
Use Technology Others Have Proven – DCI

- DCI (Data Centre Interconnect) Microsoft created the product category due to their unique application
- Now an industry standard called 400G and 800G ZR that all use



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Hyperscalers Engage Smaller, Leading Technology Companies

- Flexible and responsive - Willingness for risk - Creativity
- Many of today’s semiconductor companies' success can be traced to the development of solutions through early engagement with Hyperscalers
  - AI and compute
  - Switching
  - Module makers
  - Cable Vendors
  - Connectivity technology

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Path to Billions

- Alphawave is aggressive - Technology leadership in all forms of data movement
  - Planes, trains, and automobiles
- Business and product customised for Hyperscalers and the ecosystem
  - Will sell you just the engine or change to electric
- Delivering mission-critical connectivity and compute essential to the AI revolution

Break – Back in 20 min

ALPHAWAVE SEMI

Agenda

Welcome	Jose Cano, Global Head of IR
The Next Leader of Connectivity for AI	Tony Pialis, Co-Founder and CEO
AI and Data Centre Megatrends	Tony Chan Carusone, CTO
Silicon IP	Jonathan Rogers, Co-Founder and SVP Engineering
Path to Billions	Charlie Roach, Chief Revenue Officer
Break	
IP, Chiplets and Custom Silicon	Mohit Gupta, SVP & GM Custom Silicon and IP
Connectivity Products – Multi-Billion Dollar Market	Babak Samimi, SVP & GM Connectivity Products
Financial Overview	Rahul Mathur, Chief Financial Officer
Closing Remarks	Tony Pialis, Co-Founder and CEO
QA Session	Executive team

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IP, Chiplets and Custom Silicon

Mohit Gupta, SVP & GM Custom Silicon and IP

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Path to Billions

Leadership in Connectivity and Compute

Ultra-high-speed data connectivity for AI, compute and network architectures

ALPHAWAVE SEMI

Leadership in Connectivity and Compute

Ultra-high-speed data connectivity for AI, compute and network architectures

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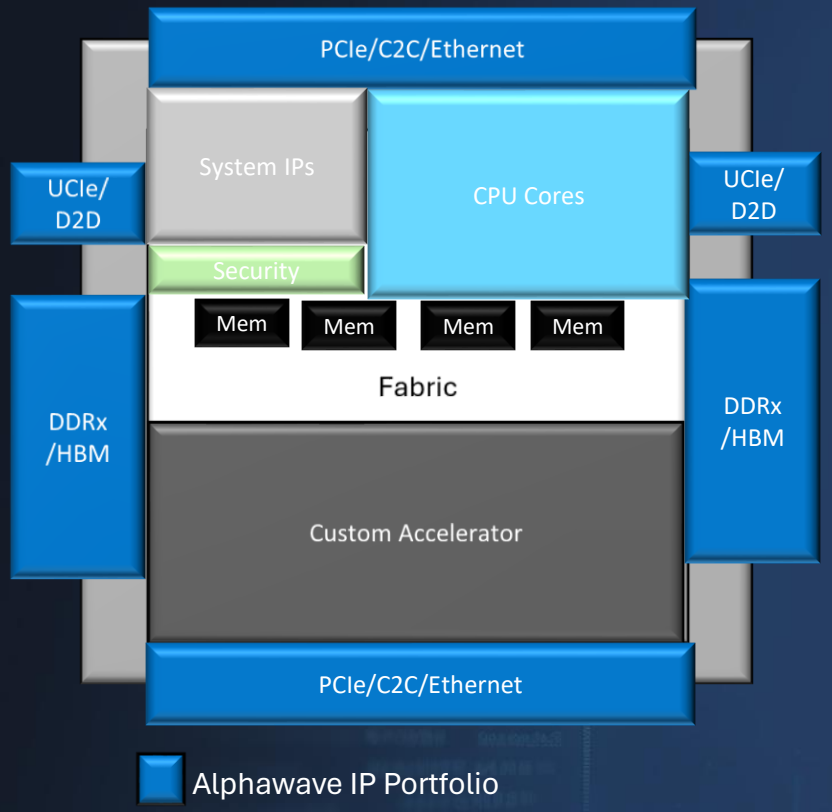
Advanced Silicon IP is Fundamental for the AI Era

AI xPUs

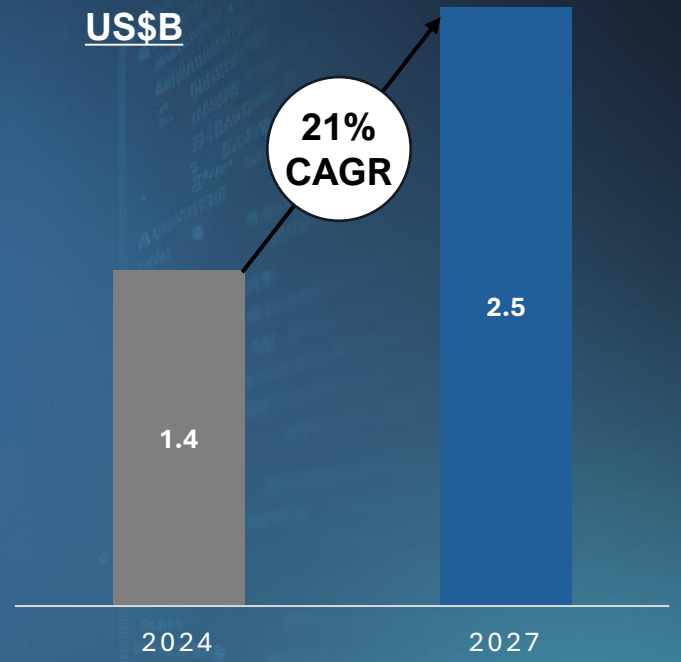


Alphawave IP Portfolio

Key Market Drivers

- Custom Workloads: New Chip Design Starts
- Faster Scaling: 5nm → 3nm → 2nm → Angstroms
- Multi Die Integration: Requires Connectivity IP

CONNECTIVITY IP TAM



IP nest, Internal Estimates

Silicon IP – High-margin business enabling standalone IP licensing & adjacent silicon revenue

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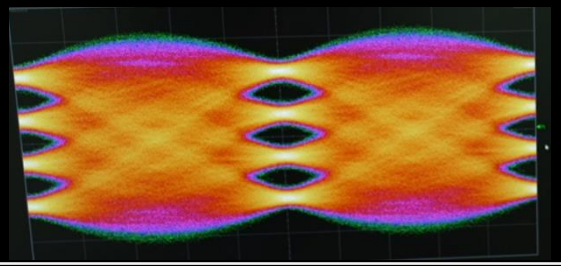
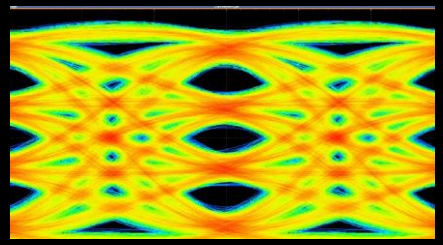
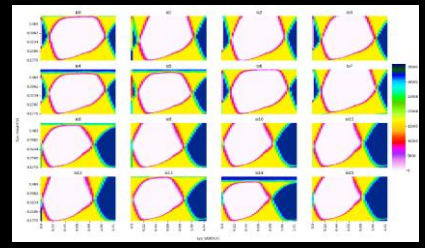
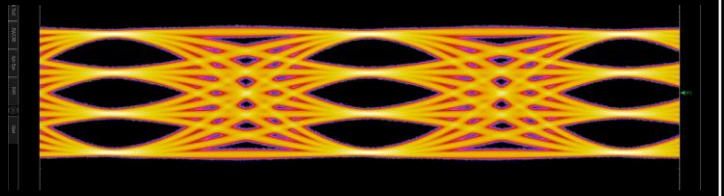
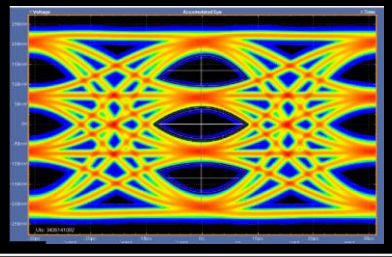
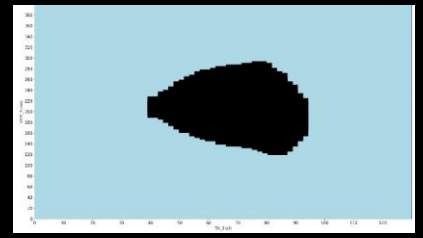
Alphawave has a Full Suite of AI Silicon IP Subsystems

		
224Gbps	128Gbps/PCIe Gen7	UCIe/D2D 24Gbps
		
112Gbps	PCIe Gen6/CXL3.x	HBM3e 9.2Gbps+

7/6nm 5/4nm 3/2nm 18/16/14A

Proven silicon IP subsystems – Lowers risk, reduces customer engineering efforts

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Alphawave has a Rich History of Silicon IP Deployment

The Alphawave team has a >20-year industry track record of delivering the most advanced IPs

ALPHAWAVE SEMI

Leadership in Connectivity and Compute

Ultra-high-speed data connectivity for AI, compute and network architectures

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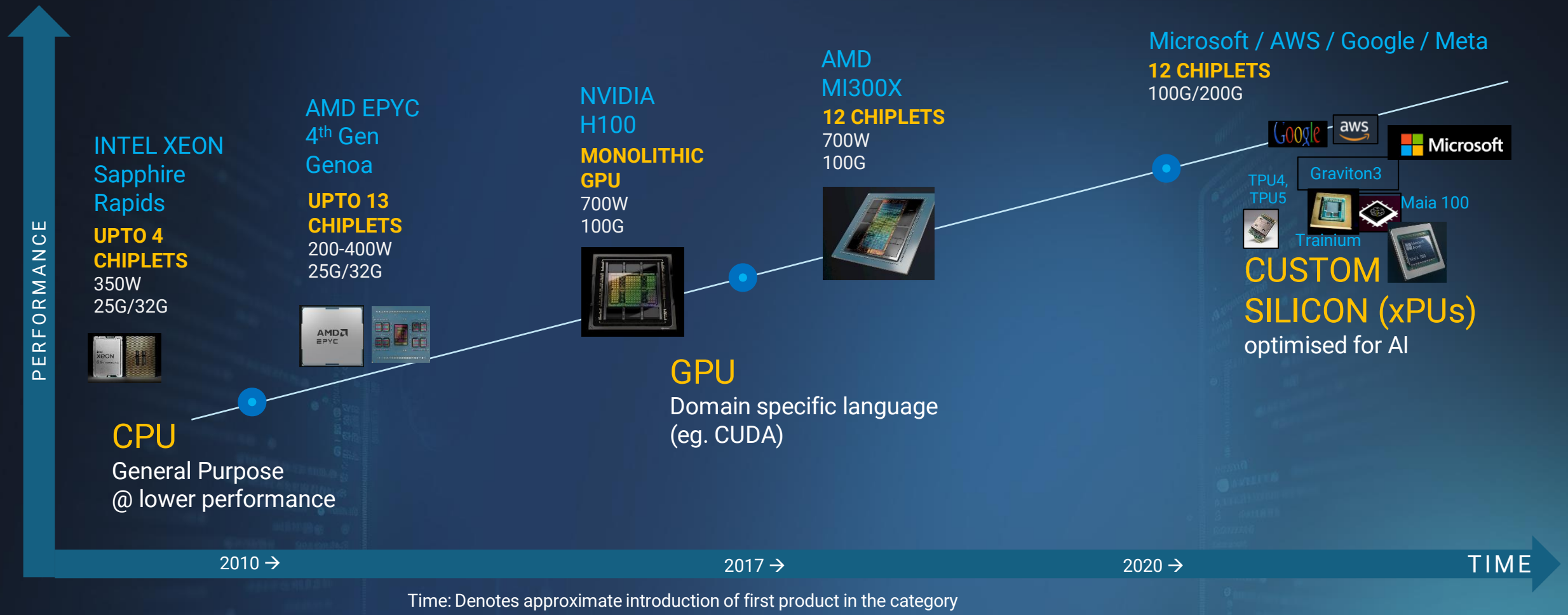
The Result: Emergence of Silicon for AI



Time: Denotes approximate introduction of first product in the category

Until now – No one solutions provider possessed all of the technology to enable silicon for AI

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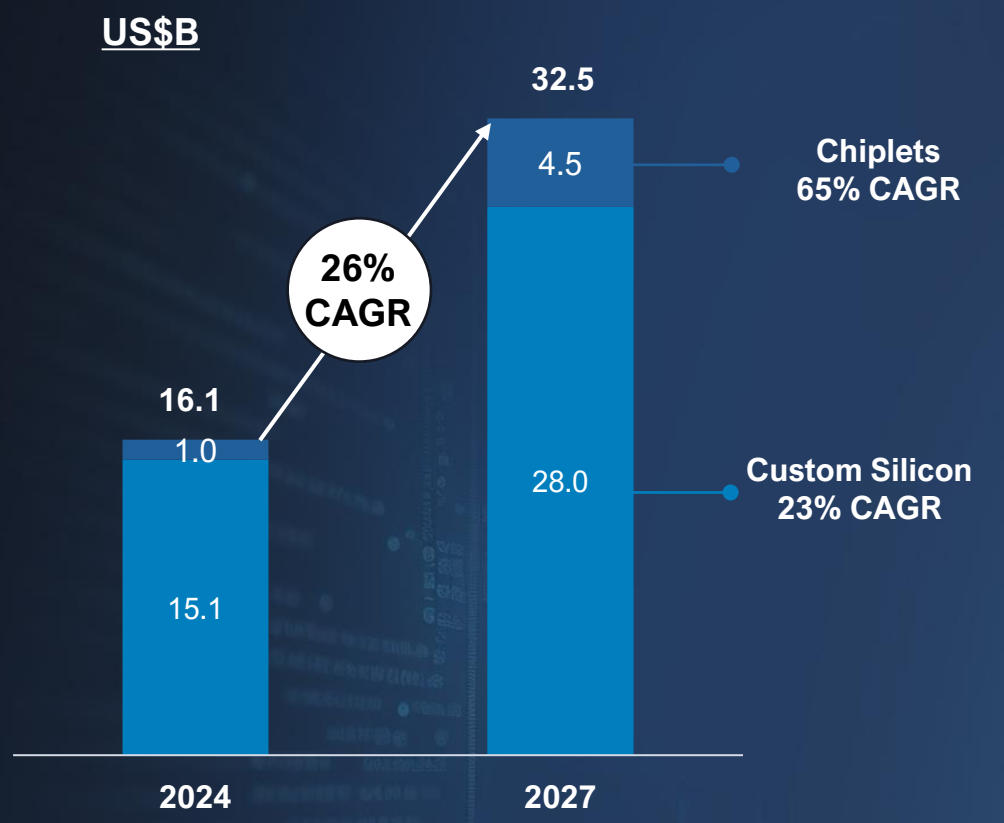
Growing Custom Silicon Market Driven by New AI Workloads



Semico Research Corporation, JP Morgan, IPNest ,LightCounting, Internal Estimates

Maximising Performance with Optimised Power for Specific Use Cases

- Purpose-built custom SoCs leveraging high-speed connectivity with increasing levels of compute
- Targeted at high-end, data centre infrastructure market segments

- Optimised to specific use cases
  - AI LLM training and inference acceleration, video streaming servers, accelerators for public cloud, etc

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Leveraging our Full Portfolio of Technologies for AI Silicon

Custom silicon and chiplet solutions optimised for AI workloads are essential to affordably scale compute and connectivity performance, achieve lower power, and faster time to market

Connectivity

Compute interfaces
PCIe 1.0-7.0
CXL 3.1+

Networking interfaces
112G/224G SerDes
Ethernet 400G/800G/1.6T

Memory interfaces
HBM3/4
DDR5 and LPDDR5/4x

Chiplet interfaces
UCIe 36G

+

Compute

High Perf. CPU Cores

ARM Total Design

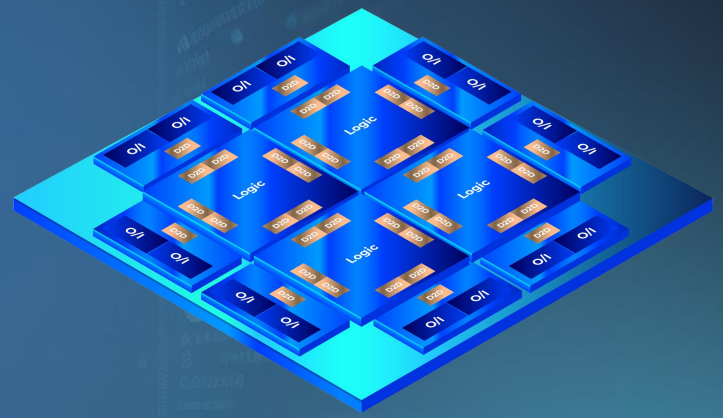
3/2nm PPA optimised

Fabric-IO latency optimised

Compute Chiplets

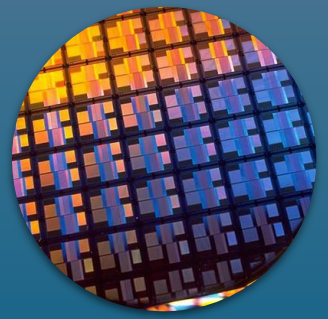
=

AI Silicon Solutions



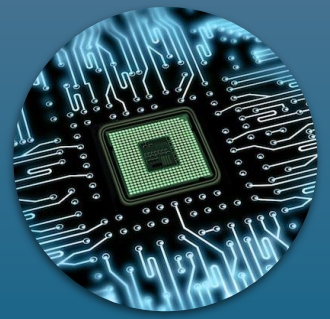
ALPHAWAVE SEMI

Alphawave's Complete Custom Silicon Platform for AI Silicon



Leading Process

- 7nm - Production
- 5nm - Ramping
- 3nm - Taping out
- 2nm - Enablement

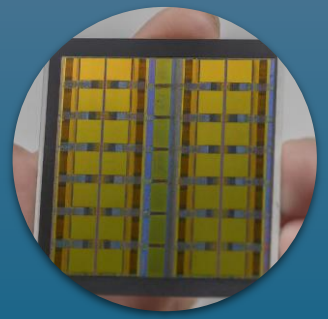


Proven Silicon IP

- 224G/112G Ethernet
- PCIe / CXL
- HBM/UCIe
- Sub-systems

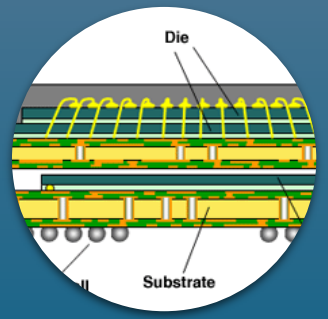
Ecosystem

- ARM Total Design
- Leading Foundries
- Design Flows
- Multi-geo OSATs



Pre-Built Chiplets

- Fast TTM
- Lower Risk
- $ savings



Adv. Packaging

- 2.5D/3DIC
- SI/PI
- Mechanical/Thermals

Significant R&D investments to enable long-term silicon revenues

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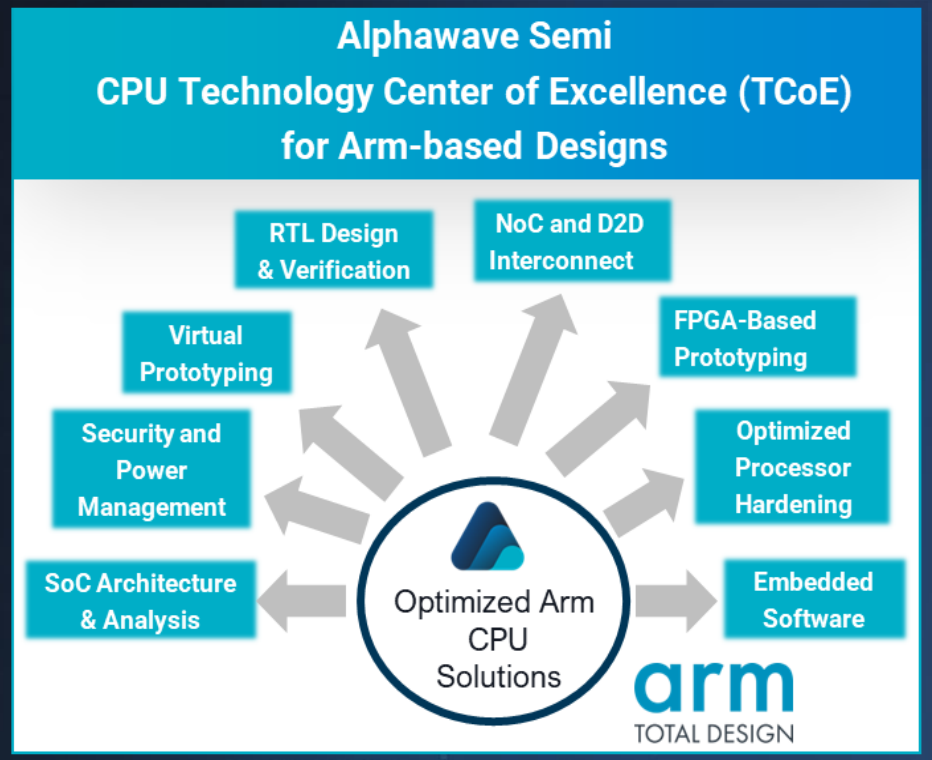
Driving Partnership: Leveraging ARM to Enable AI xPUs



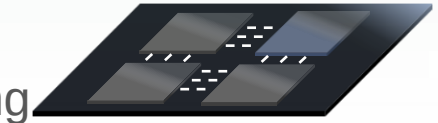
- Alphawave Semi joined as a founding IP and Custom Silicon member
- Provides accelerated path for specialised SoC solutions based on ARM Neoverse Compute Subsystems (CSS)
- Multiple ARM cores in production optimised for performance, power and area (PPA)
- Our connectivity IP seamlessly complements ARM IP
  - Supports ARM fabric interfaces such as AXI and CHI/CXS
  - Enables easy integration of advanced connectivity such as PCIe/CXL, HBMx, DDRx, Ethernet and UCIe

Chiplets – Next Evolution of Silicon IP

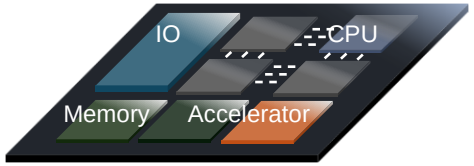
New Chiplet Design Paradigm

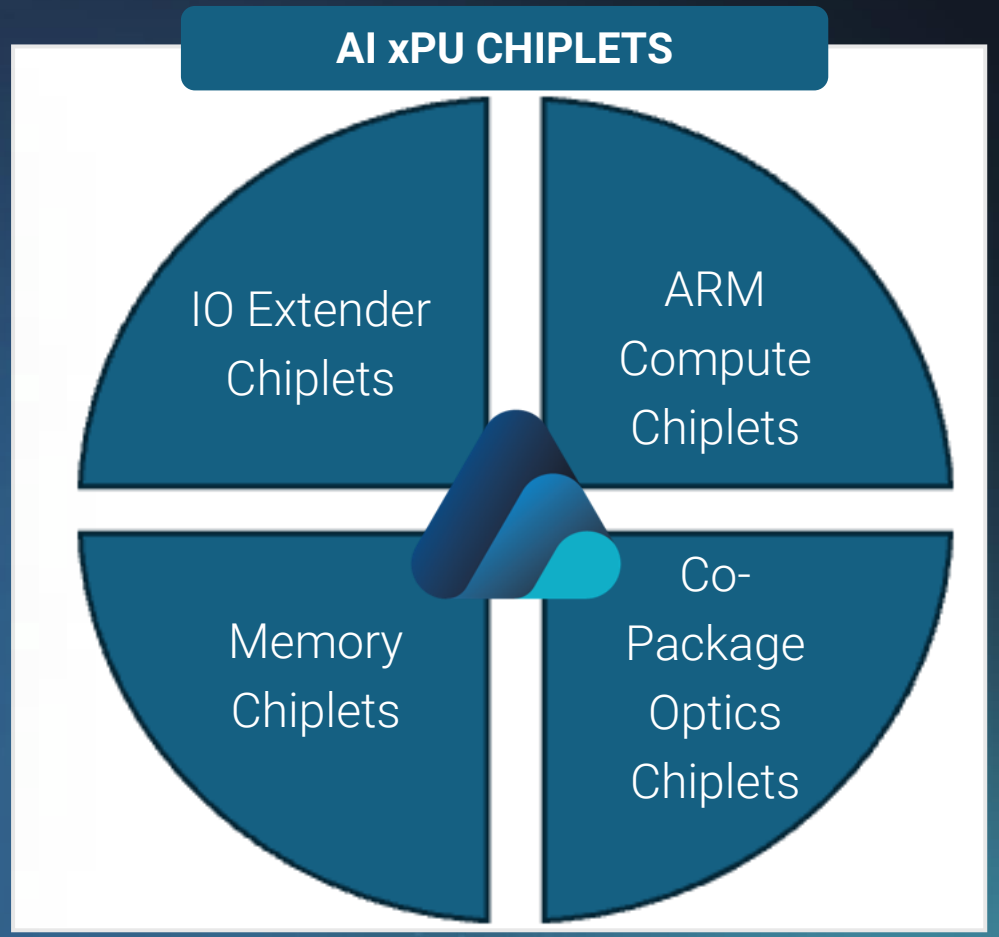
Monolithic is costly for AI and Data Centre in 3/2nm nodes

Chiplets with 2.5D/3DIC allow for greater compute and memory scaling



Customisable IO and Compute Chiplets Accelerate Time to Market





Partnering with ARM to deliver a portfolio of Neoverse series compute and IO chiplets

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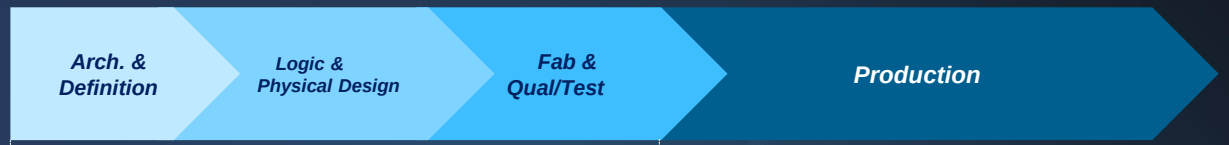
Scaled Acceleration for AI xPUs with Chiplets

1

Time to Market Advantage

30-50% Development time savings

Monolithic

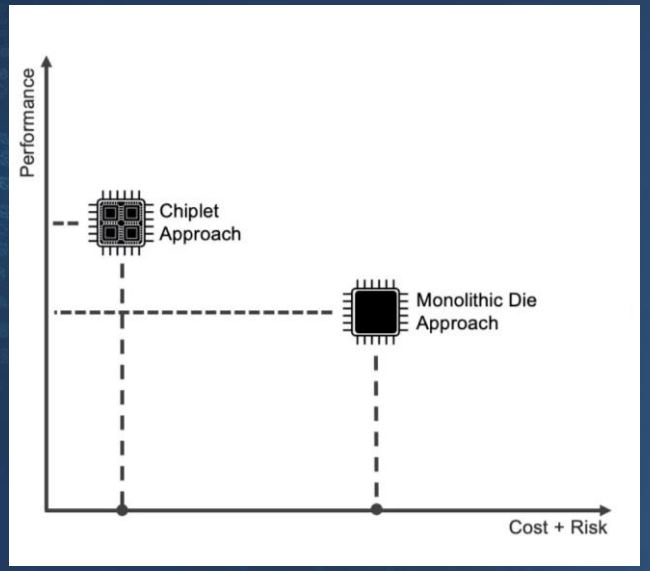


Chiplet-Based

2

Lower Risk/Cost

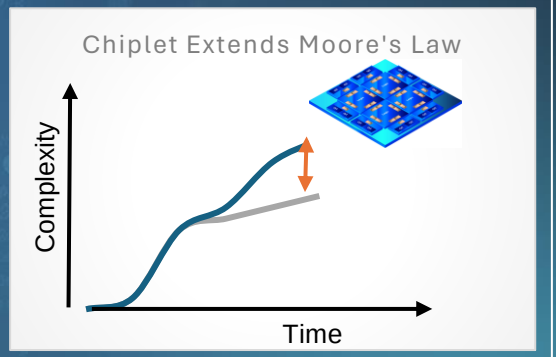
30-50% Cost savings



3

Accelerated Compute

Extends process scaling



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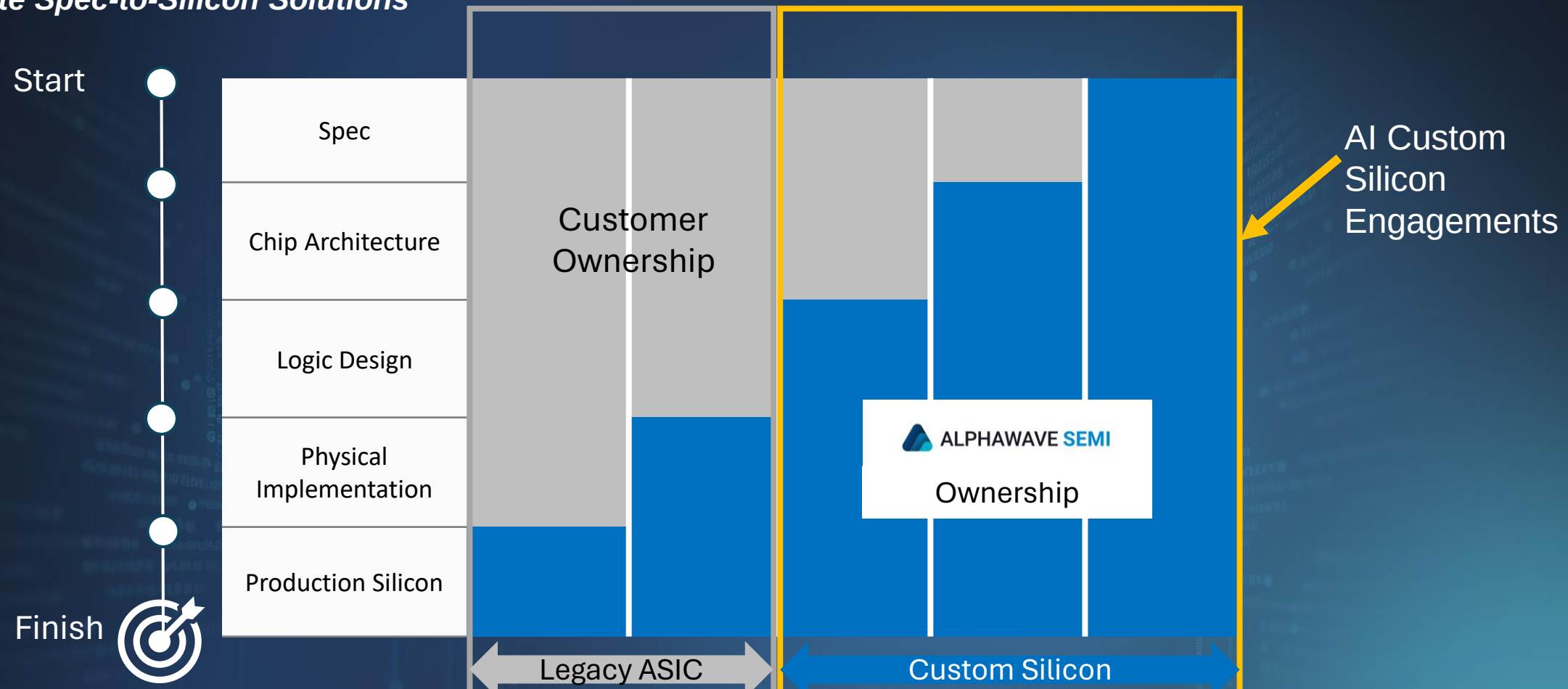
Delivery Through Flexible and Valued-Added Business Model

Complete Spec-to-Silicon Solutions



ALPHAWAVE SEMI

Alphawave Already has Custom AI xPUs Design Wins *Today*

CHIPLET-BASED AI ACCELERATOR CHIP

Customer-provided accelerator IP

Alphawave portfolio of IP: UCIe/PCIe/Ethernet/HBM3e subsystems

4x main dies + 8 HBM3e

ARM NEOVERSE-BASED HPC CHIP

ARM compute subsystem

HBM3e/DDR/PCIe/UCIe subsystems

2x main dies + 4 HBM3e

MONOLITHIC AI ACCELERATOR CHIP

Performance opt. reticle size chip (>800 sqmm)

HBM3e/112G/PCIe subsystem

1x main die + 6 HBM3e

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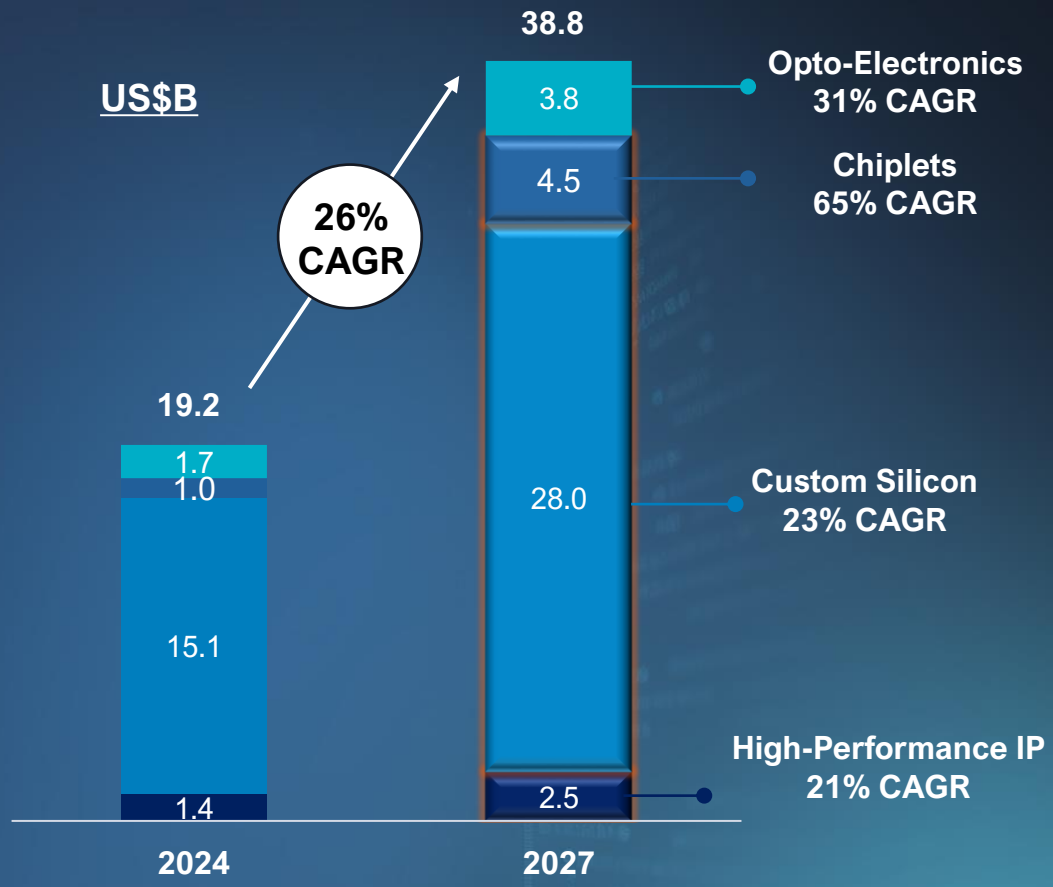
Execution Against a Massive Market Opportunity

- Generative AI “GenAI” driving the need for specialised silicon ~ $35B market opportunity
- Early investment in process and IP enables a differentiation for long-term custom silicon revenue
- Initial success with xPU design wins across worldwide customer base
- Well positioned to deliver complex AI silicon leveraging Internal IP, chiplets and access to industry leading ecosystem



Semico Research Corporation, JP Morgan, IPNest ,LightCounting, Internal Estimates

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Connectivity Products

– Multi-Billion Dollar Market

Babak Samimi, SVP & GM Connectivity Products

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Leadership in Connectivity and Compute

Ultra-high-speed data connectivity for AI, compute and network architectures

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Intersection of GenAI and Accelerated Compute: Connectivity

GPU Capacity Outpacing Connectivity Bandwidth

GenAI Megatrends Disrupting Connectivity Market

- Catalyst for faster transition to 200G PAM4 (1.6T transceivers)
- More optical ports: Each GPU = 3+ transceiver attach rate
- Distributed AI: 20km Coherent-Lite DCI links now in focus
- Power/Energy: Necessitates move to 3nm now→ 2nm for NGen

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We Own the Critical Connectivity Assets

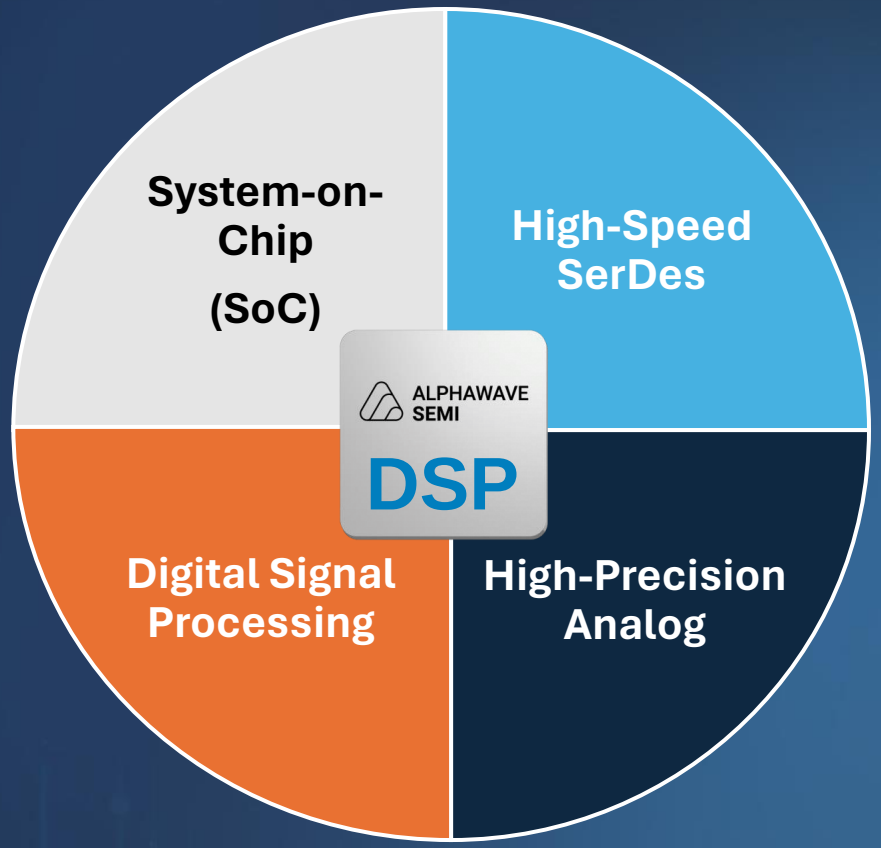
DSP is the processor to connectivity like GPU is the enabling processor of GenAI

Optics + Analog + Digital

SoC + Firmware

PAM4

Coherent



112G, 224G → 400G

4nm, 3nm → 2nm

ADC / DAC[1]

>120G Baud

WidEye™ DSP - Innovation Powering Our Differentiation

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[1] Analog to Digital Conversion / Digital to Analog Conversion

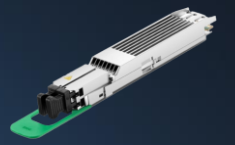
Building Connectivity Solutions for GenAI Data Centre

AEC

AOC

400G

800G



1.6T

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Electrical DSP PAM4

2m+

ALPHAWAVE SEMI

Optical DSP PAM4

Up to 10km

ALPHAWAVE SEMI

Optical DSP Coherent-Lite

10km+

- **Delivering to Hyperscalers' diverse optical and electrical applications**
- **Executing in leading edge 4nm, 3nm, soon in 2nm process nodes**

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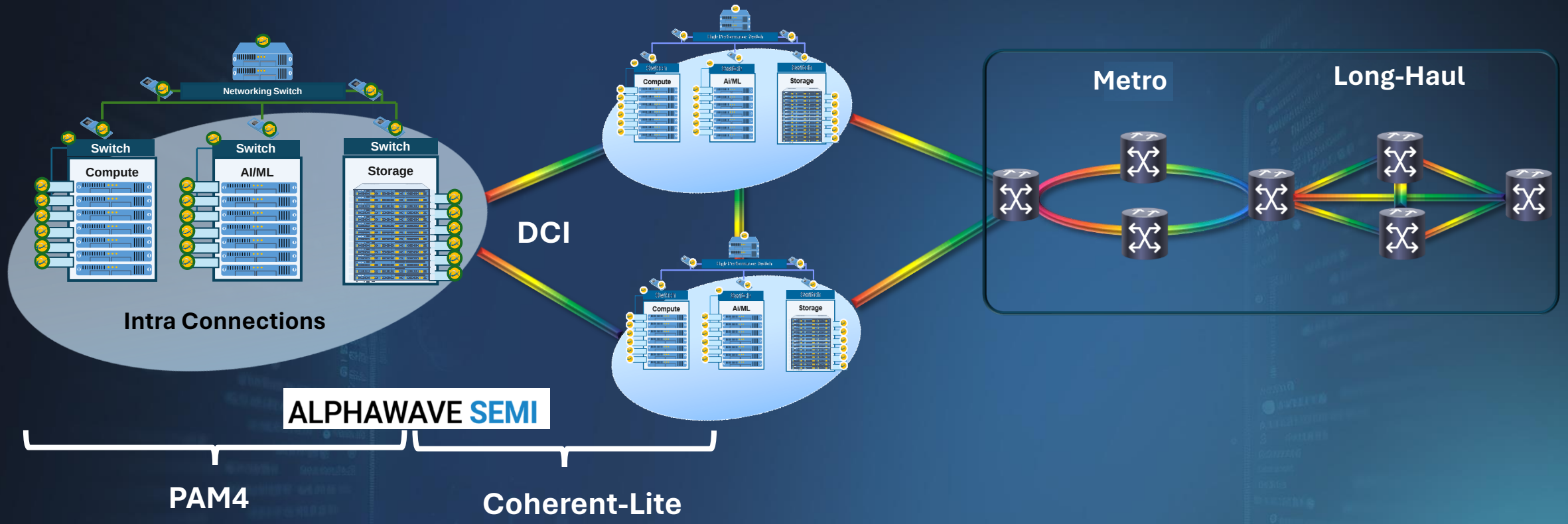
Rapidly Growing Market Opportunity for Alphawave

Coherent-Lite Solves Bandwidth Gap for up to 20km Links



PAM4 and Coherent-Lite will coexist from 1.6T to 3.2T market inflections

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Scaling our Layered Connectivity Products

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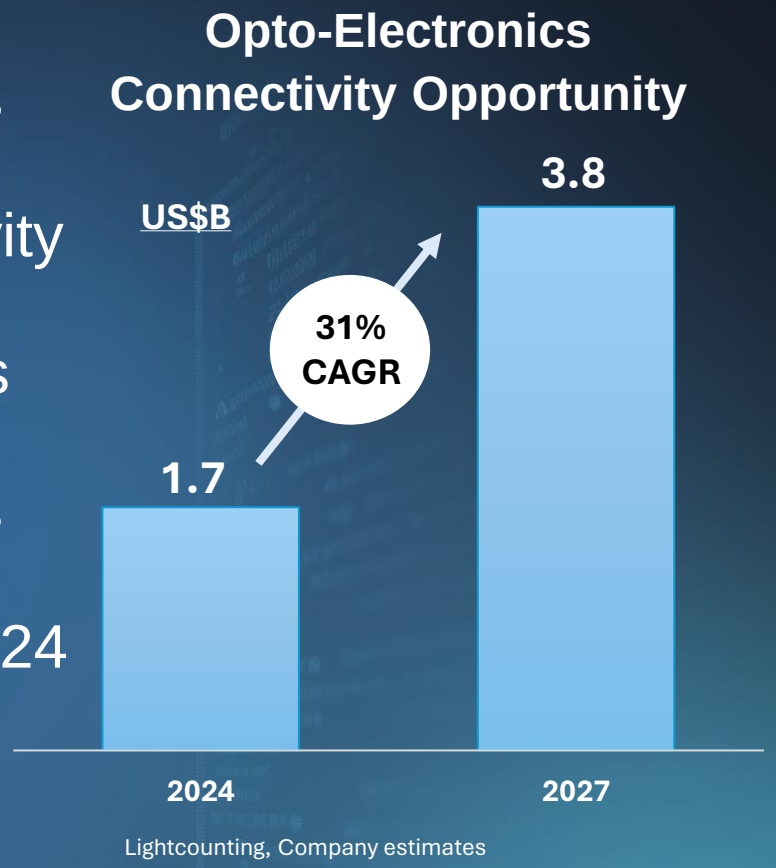
Massive Opportunity: Connectivity Products

- ~$4B TAM for GenAI connectivity now addressable by us
- Hyperscalers seeking diverse supplier base for connectivity
- Uniquely positioned – have both PAM4 & Coherent DSPs
- Own all critical Analog, SerDes & DSP technology assets
- Secured initial purchase order with first revenue in 2H-2024



We have already won a >$300m multi-year agreement with leading Hyperscaler

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Financial Overview

Rahul Mathur, Chief Financial Officer

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Leadership in Connectivity and Compute

Ultra-high-speed data connectivity for AI, compute and network architectures

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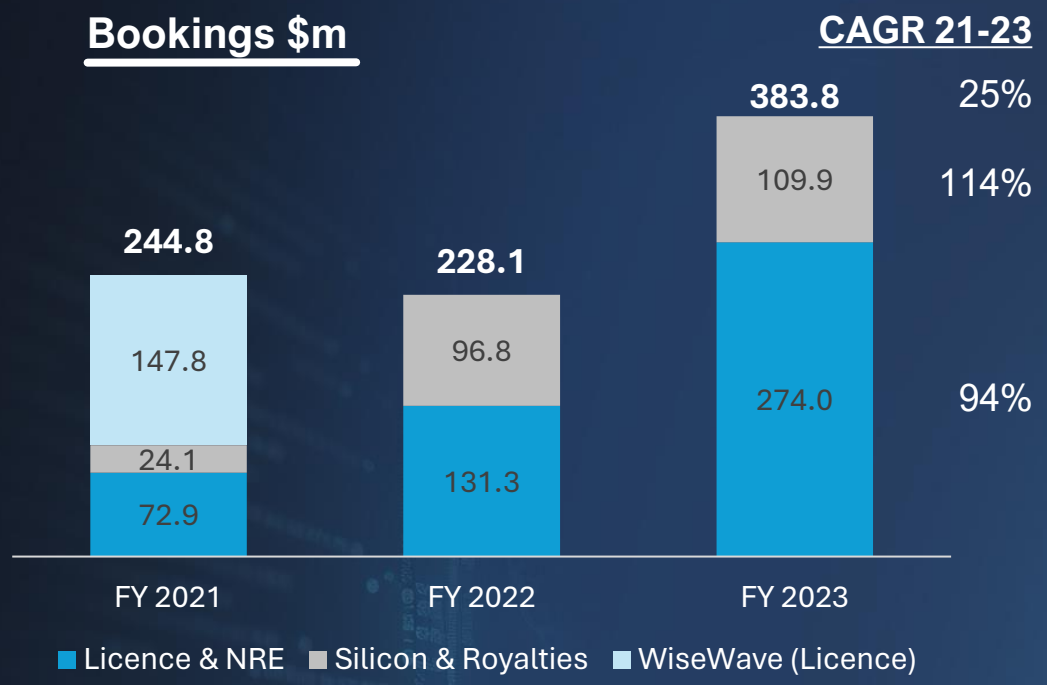
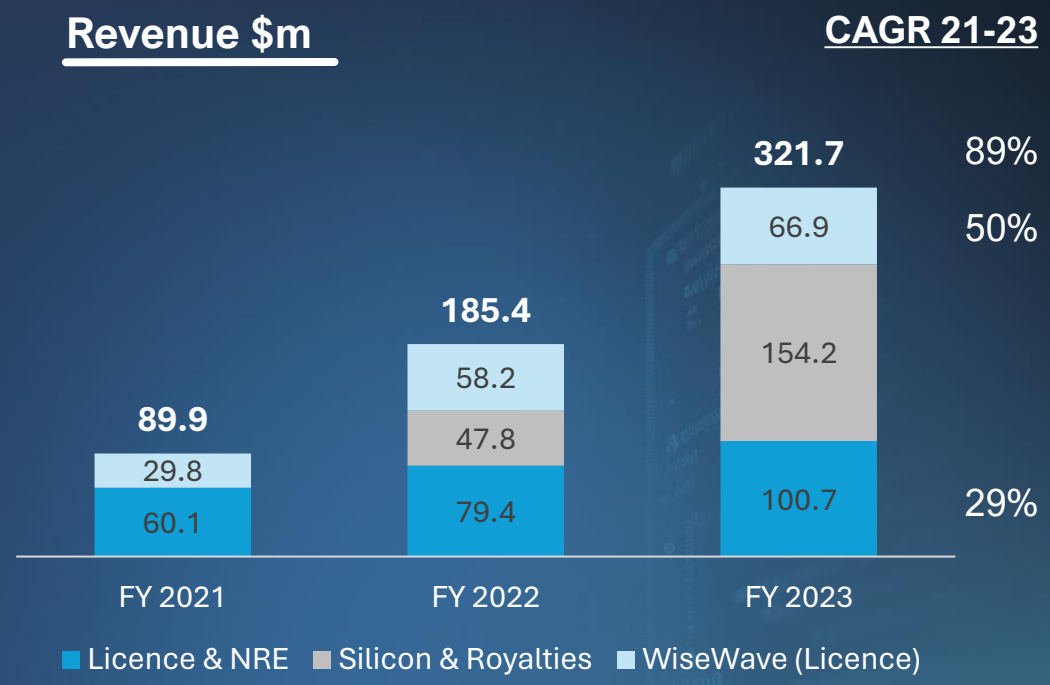
We See Strong Growth in our End Markets in all Business Areas





- Bookings trend in all business areas supports long-term revenue growth
- Transitioning Custom Silicon to higher-margin non-China business
- Delivery of WiseWave SLA in FY23 sets stage for predictable growth

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Strong FY23 Ending Backlog of $355M Supports Long-Term Growth

Timing of Cash Inflows/Outflows and Revenue Recognition Determined by Business Model

Licence & NRE[1]

Revenue recognised over development period on percentage of completion basis

- Typical pay-per-use IP licence US$5m-US$10m

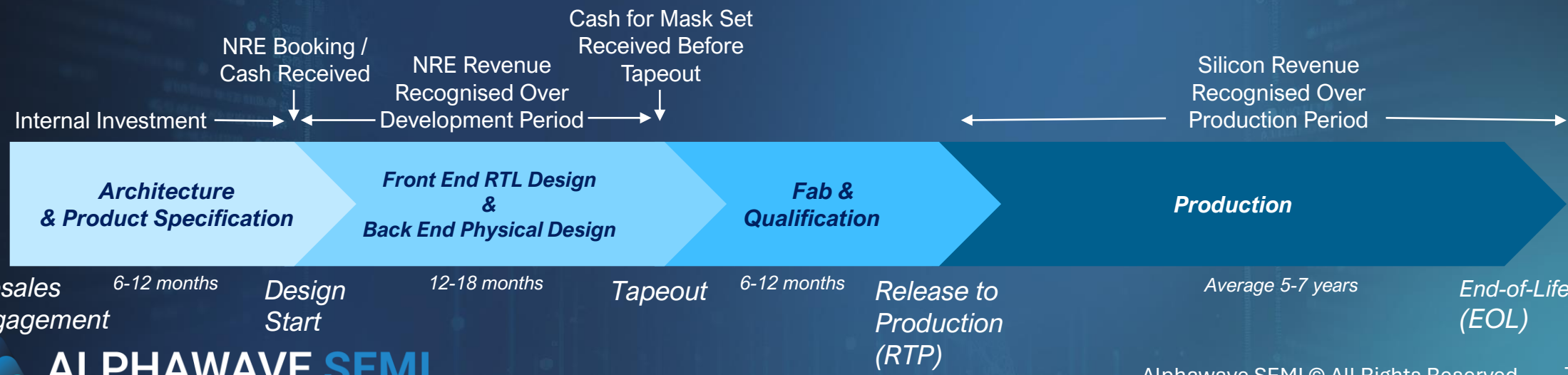
($m)	2023	2022
Bookings	$274.0	$131.3
Revenue	$167.3	$137.6
Ending Backlog	$294.8	$255.1

Silicon & Royalties

Revenue recognised on shipment

- Typical opportunity US$50m+
- ~$500m+ long-tail of silicon revenues not included in backlog
- Expect first Connectivity Products revenue in 2024

($m)	2023	2022
Bookings	$109.9	$96.8
Revenue	$154.2	$47.8
Ending Backlog	$60.1	$124.6



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Continued Investment in Profitable Growth Drives Key P&L Metrics

US$m	FY 2023	FY 2022	Change	Comments
Revenue	**321.7**	185.4	74%	Growth with North American and APAC customers. Significant contribution from legacy OpenFive backlog.
Gross profit	**165.4**	124.6	33%	Change in business mix from delivery of OpenFive legacy backlog
Gross margin	***51%***	*67%*	*(16)ppts*	
R&D, S&M, G&A	**(131.8)**	(89.5)	47%	Annualised impact of increased headcount from the 2022 acquisitions and ongoing investment in the business to support growth
Adjusted EBITDA	**62.6**	46.8	34%	
Adjusted EBITDA %	***19%***	*25%*	*(6)ppts*	
Other expenses	**(52.9)**	2.5	nm	Share based payments increased year-on-year with increased headcount; substantial exchange gains in 2022
Depreciation and amortisation	**(29.1)**	(11.7)	150%	Annualised impact from assets acquired and additions

Due to rounding, numbers presented in the chart may not add up to the totals provided.

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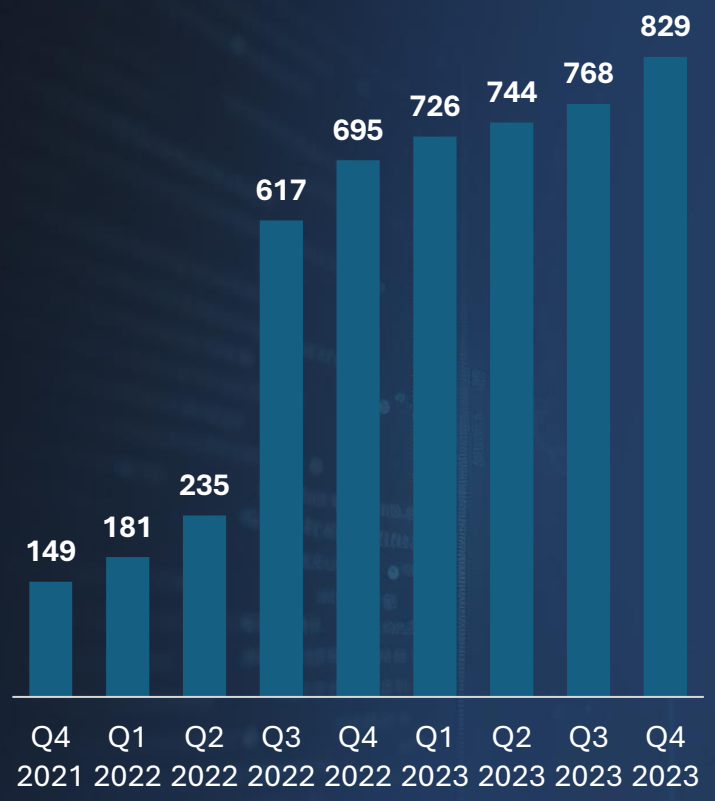
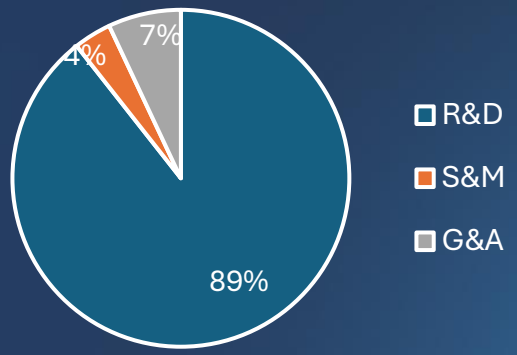
Investment Into R&D Extends Technology Leadership

Technology-Led Organisation – 89% Employees in R&D / Engineering

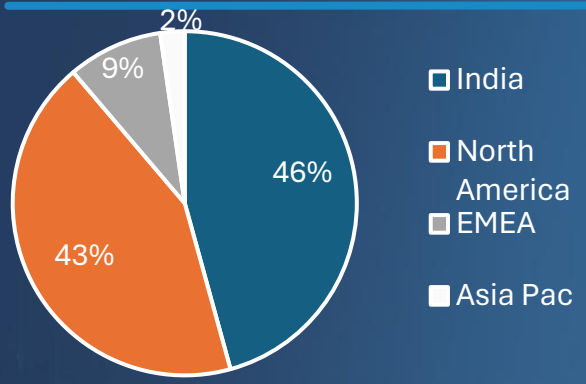
Number of Employees



By Function[1]



By Region[1]



[1] Due to rounding, percentages may not precisely reflect the absolute figures

- Focus on critical hires to support growth opportunities
- Targeting ~10% headcount growth in 2024
- US$54.5m development costs capitalised in FY 2023 (FY 2022: US$7.2m)

Main Locations

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Management of Balance Sheet and Cash Flow: Finance Priorities

US$m	FY 2023	FY 2022	Change	Comments
Cash & Cash Equivalents	**101.3**	186.2	(84.9)	Actively managing cash; low inventory and receivables balances
Loans and Borrowing	**220.4**	210.2	10.2	Attractive debt facility in place
Net Debt	**(119.1)**	(24.0)	(95.1)	Perpetually evaluating capital structure
Cash from Operations	**16.0**[1]	1.0[2]	15.0	Not dependent on additional non-operating inflows
Working Capital Changes	**(51.3)**[1]	(50.1)	(1.2)	Expect improvement in FY24 working capital
Capital Expenditures	**18.6**	4.2	14.4	Expect increase in FY24 CapEx for facility build outs
R&D Capitalisation	**43.7**[1]	7.2	36.5	Significant investment in future products support long-term growth opportunity

1 Restated to reflect capitalisation of interest incorrectly included in both interest paid and capitalised development expenditure in the FY23 cash flow statement.
2 Excluding US$28m deferred compensation payments related to acquisitions
Due to rounding, numbers presented in the chart may not add up to the totals provided.

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Our Mid-Term Model and Guidance: Driven Bottom-Up

US$	2024	2025
Revenues	$345-365m	$450m
Gross margin	c.50%	c.50%
Opex %	c.30%	c.25-30%
Adjusted EBITDA[1]	Approx. $70m	Approx. $100m
Adjusted EBITDA %	c. 20%	c.20-25%
Capex (exc. Cap R&D)	c. 10%	c. 10%
Cap. R&D	~$50-60m	~$50-60m

- 2023-2025 revenue CAGR of ~20%
- We expect the revenue profile in 2024 to be back-end loaded and H1 2024 revenue to be below H1 2023, which saw a significant contribution from the legacy OpenFive backlog
- In H1 2024, we expect to invest in capital and R&D expenses as we continue to invest in our product business
- 2024 Capex increase driven by investment in own products

1 2024 assumes mid-point of the guidance range and 20% adjusted EBITDA margin; 2025 assumes US$450m revenue and 20-25% adjusted EBITDA margin

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Alphawave Growth in 2024 and Beyond

- Delivering mission-critical connectivity and compute essential to the AI revolution
- Addressing the insatiable demand from hyperscalers and world's leading semiconductor companies through:
  - Silicon IP
  - Custom silicon
  - Chiplets
  - Connectivity products
- Future growth fueled by disciplined investment in R&D for high-margin products

Powering the AI Revolution = Path to Billions

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Leadership in Connectivity and Compute

Ultra-high-speed data connectivity for AI, compute and network architectures

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Appendix

Non-GAAP Metrics

See Notes 4 to the Consolidated Financial Statements Alternative Performance Measures H1 2023 Interim Report and FY 2023 Annual Report at https://www.awaveip.com/en/investors/results-reports-presentations/

- Bookings are a non-IFRS measure representing legally binding and largely non-cancellable commitments by customers to license our technology. Our bookings comprise licence fees, non-recurring engineering support and, in some instances, our estimate of potential future royalties. A portion of our bookings may not convert to revenue if those royalties do not materialise or customers are unable to pay us.
- Backlog is a non-IFRS measure representing our bookings less revenues recognised to date. It represents the revenue that we expect to collect in future years based only on our existing and legally binding orders. As new bookings are secured, our backlog will increase and as existing bookings are recognised as revenue, our backlog will decrease.
- Adjusted EBITDA is a non-IFRS financial measure defined as the Group's earnings before interest, taxation, depreciation and amortisation, adjusted to remove share-based payment charges and non-recurring operating expenses such as IPO-related costs (in 2021) and advisory costs associated with acquisitions. Adjusted EBITDA is reconciled in note 4 Alternative performance measures (APMs).